THE ANALYSIS, DESIGN, AND FABRICATION OF A VARIABLE FREQUENCY "NOVEL" DISTRIBUTED PARAMETER FILTER

A Thesis

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of the Requirements for the Degree

Master of Electrical Engineering

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by

Harry Francis Benz

June 1970

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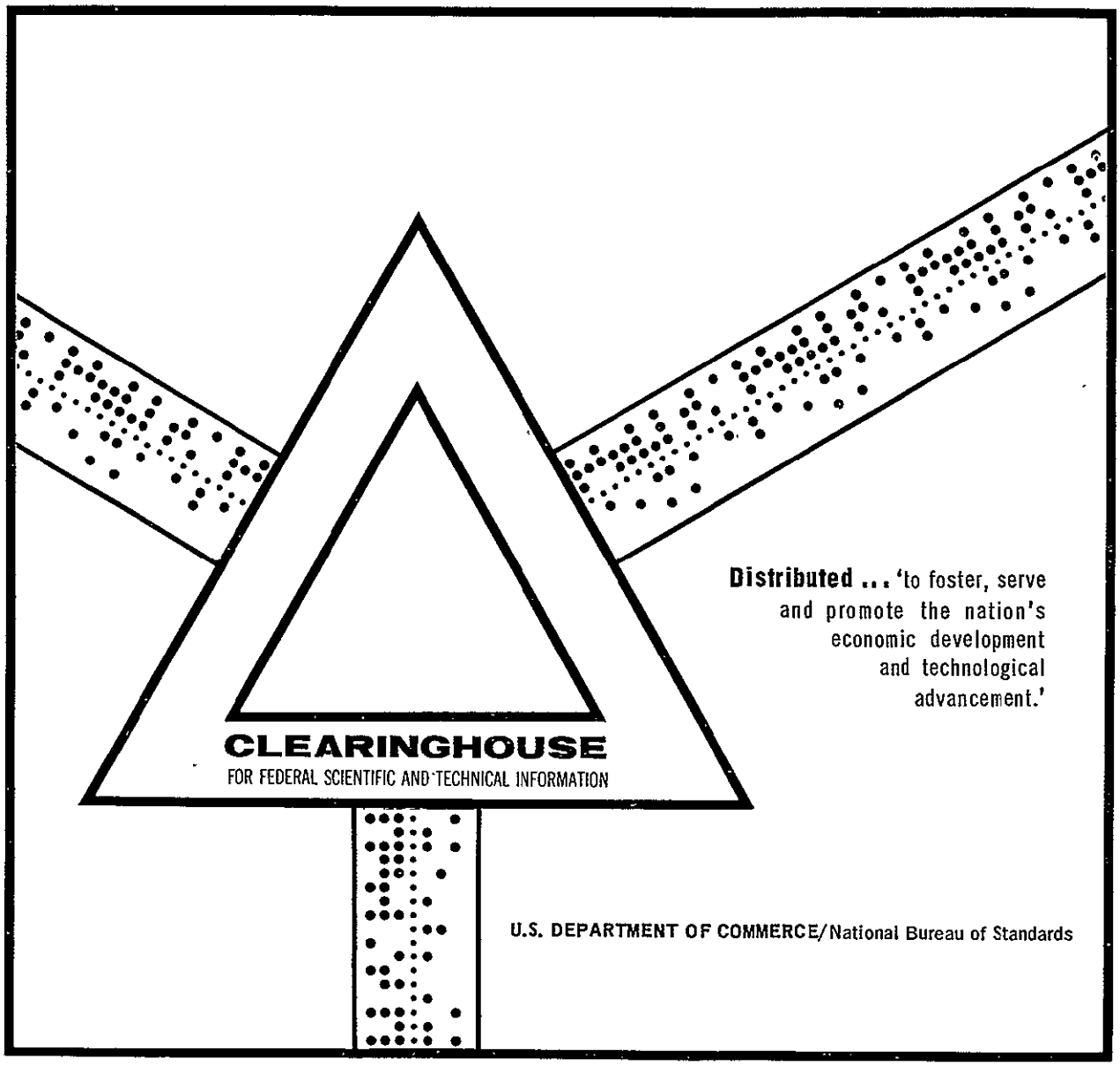

APPROVAL SHEET

This thesis is submitted in partial fulfillment of

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Author

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ABSTRACT

A new distributed parameter "novel" null device has been designed, simulated, and fabricated. It is based on Kaufman's "Novel" Null Device, but has the added feature of tunability. Tunability is implemented by considering the two elements of Kaufman's filter as distributed variable resistors and implementing them with MOS-FET's.

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LIST OF SYMBOLS

A	a surface area
Å	angstrom unit = 10^{-10} meter
C	total capacitance of series element
$\mathcal{C}$	a generalized capacitance
C_{GC}	capacitance between gate and channel of a MOS-FET
C_{CS}	capacitance between channel and substrate of a MOS-FET.
c_o	capacitance per unit length
C_{ox}	capacitance per unit area of the gate oxide of a MOS-FET
^oC	degree centigrade
d	length of the uniformly distributed RC line
D	length of the shunt MOS-FET channel
E_{in}	potential across input terminals of network
E_{out}	potential across output terminals of network
f_{null}	the desired null frequency (in Hertz)
g	transconductance of a MOS-FET
H(s)	transfer function of network
I_{in}	current flowing into input terminals of network
j	$\sqrt{-1}$
Khz	kilohertz
l	the length of a current carrying resistive element
Mhz	megahertz
mil	10^{-3} inch
MOS-CV	metal oxide semiconductor capacitance versus voltage
MOS-FET	metal oxide silicon field effect transistor

MΩ	megohm
N_A	number of acceptor impurities per unit volume
pf	picofarad
R	total resistance of series element
$\mathcal{R}$	a general resistance
R-C	resistance capacitance
r_o	resistance per unit length
R_x	resistor used in derivation of null effect
s	Laplace variable
t	thickness of a layer
torr	pressure expressed in millimeters of mercury
URC	uniformly distributed RC line
V_A	bias of series MOS-FET with respect to the substrate
V_B	bias of shunt MOS-FET with respect to the substrate
V_G	gate voltage of a MOS-FET with respect to the substrate
V_T	turn of voltage of a MOS-FET
VCVS	voltage controlled voltage source
w	width of the series MOS-FET channel
W	width of the shunt MOS-FET channel
Z	impedance
Z_o	characteristic impedance of uniformly distributed RC line
Z_{URC}	total impedance of a uniformly distributed RC line
$Z_1, Z_2, Z_3, Z_4, Z_{11}, Z_{12}, Z_{21}, Z_{22}, Z_{series}, Z_{shunt}$	impedance of null network
α	a pure number which is derived equal to 17.7985

γ	a frequency variable equal to $\left(\frac{\omega}{\omega_1}\right)^{1/2}$
Γ	transmission coefficient of a uniformly distributed RC line
ϵ_o	permitivity of free space
$\epsilon_{silicon}$	the relative permitivity of silicon
ϵ_{SiO_2}	the relative permitivity of silicon dioxide
μ	micron = 10^{-6} meter
μ_n	mobility of an electron
$\mu(\omega)$	a complex frequency variable
ρ	bulk resistivity
ρ_s	surface resistivity
ω	frequency variable
ω_1	a fixed radian frequency of a particular network
ω_{null}	the desired null radian frequency

CHAPTER I

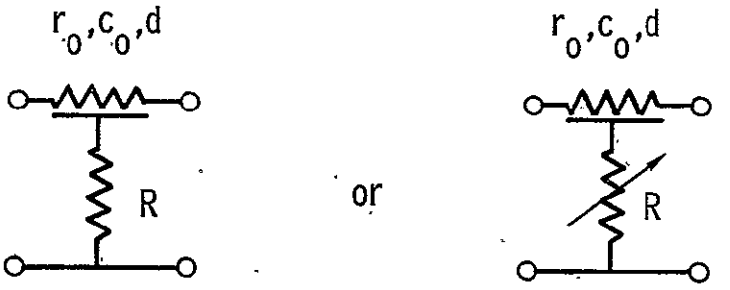
INTRODUCTION AND THEORETICAL PRELIMINARIES

Introduction

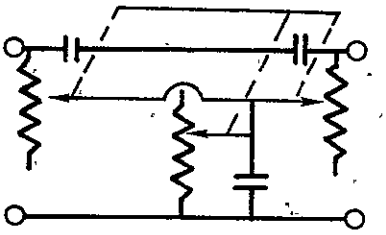
A "novel" distributed parameter notch filter was first described in 1959 by W. M. Kaufman.[1] Figure 1(a) is a schematic sketch of his distributed R-C series element with its shunting resistor. He adapted his distributed network from the standard bridged-tee type of null network. An early source reference for the bridged-tee null network is Scott[2] who proposed such a selective circuit in 1938. Figure 1(b) is a schematic sketch of Scott's twin-tee. Kaufman fabricated his "novel" distributed network in both the thick film screened regime, and on a large geometry silicon substrate. This type of null device has been used in many types of selective circuits, both as filter and as feedback element in oscillators and selective amplifiers. Kaufman's circuit does, however, have one fundamental limitation in that it is fixed in frequency and this frequency is fixed rigidly by the construction employed. The frequency can be varied slightly if the shunting resistor is varied, but this technique also limits sensitivity. Many suggested improvements have been made for this type of filter to improve its tunability while still maintaining it selectivity. One such improvement is suggested by Wyndrum[3] and is included as Figure 1(c). In it, he proposes essentially a variable resistor and a variable capacitor in the shunt leg of the filter. This does improve the tunability while maintaining selectivity, but it is not a single adjustment;

it is a pair of matched adjustments, the adjustments being mechanically done and in addition, these adjustments are limited over a specific tuning range. Another modification is described by Golembeski[4] drawn as Figure 1(d), in which he proposes tuning the device by using one fixed resistor in parallel with the distributed R-C element, and one variable "shunt" leg resistor. This network is tunable over limited frequency ranges. Roy and Shenoi[5] describe several notch networks using distributed R-C elements. The R-C configurations that they demonstrate are presented as Figure 1(e-j). Another modification is patented by Medwin.[6] His modification of the network is presented as Figure 1(k) and he essentially uses a bridged-tee configuration of a split channel Metal Oxide Silicon Field effect Transistor (MOS-FET), which is still limited in variability over a range of approximately 7 to 30 Mhz. A final modification has been patented by Evans,[7] which is not redrawn. In it Evans uses fixed capacitors and two variable resistance MOS-FET's in a standard configuration to approximate an R-C filter, where no distributed effects are considered.

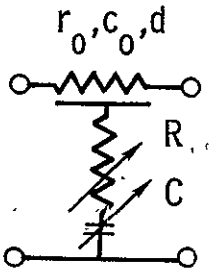
This thesis addresses itself towards a further improvement of Kaufman's type filter with two distinct advantages. This improvement will make the filter tunable electronically over a wider range than has been available and it will result in a circuit which is compatible with the silicon planar technology. Essentially, the improvement is to consider the large geometry MOS-FET as a distributed element in Kaufman's filter regime. That is, to use the gate to channel resistance as a distributed resistor as shown in Figure 1(l). If now, two such devices



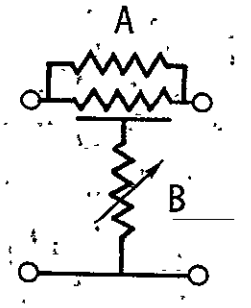
(a) Kaufman's distributed RC novel notch network.



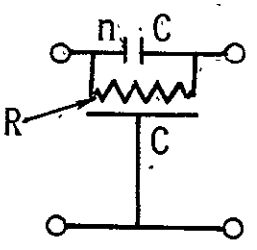
(b) Scott's twin tee.



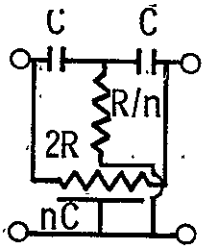
(c) Wyndrum's improvement of Kaufman's filter.



(d) Golembeski's tuning method.

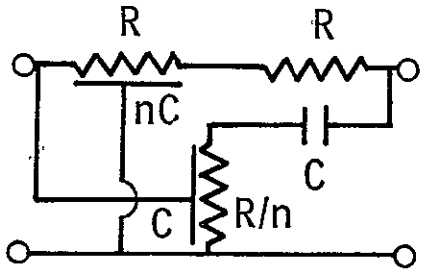


(e)

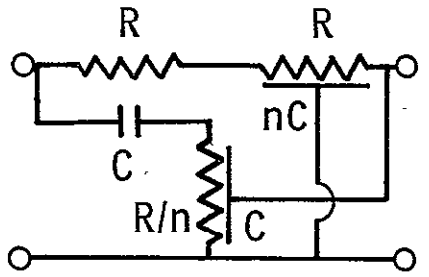


(f)

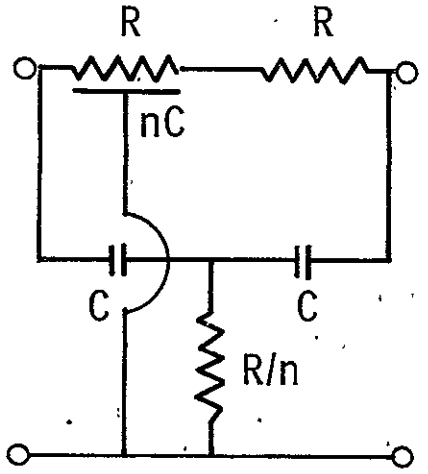
Figure 1.- Distributed RC null devices.



(g)

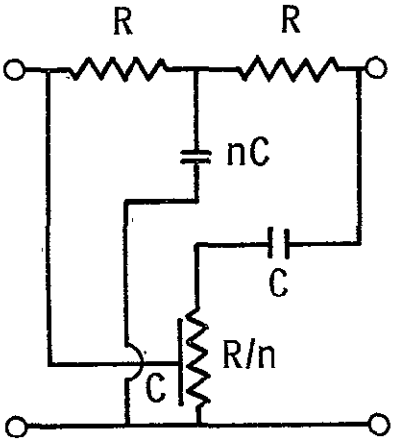


(h)

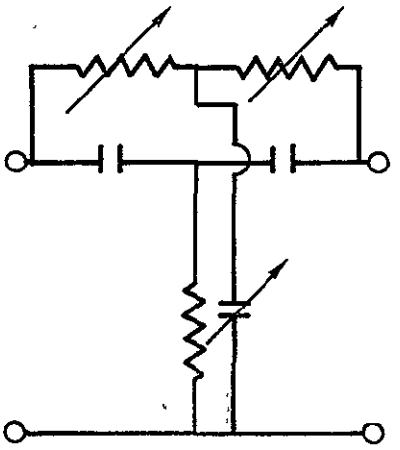


(i)

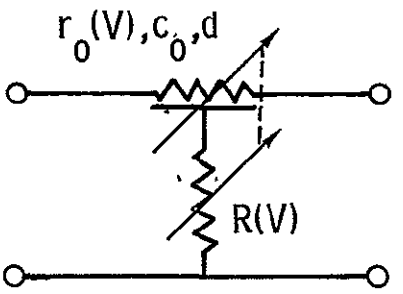
Figure 1.- Continued.



(j)



(k) Medwin's improvement of Kaufman's null network.



(l) Tunable notch network.

Figure 1.- Concluded.

are fabricated as a pair, the channel resistances per unit length may be forced to vary together with bias in a fixed ratio which will force continuous tuning over a wider range.

This device pair is drawn in cross section in Figure 2. The pair demonstrates that two MOS-FET's are used as the distributed and control devices. They are the insulated gate n-inverted channel type and are to be fabricated on p-substrates. The principles involved do not necessarily restrict the concept to this regime, but this is the approach that has been adopted. That is, these devices could be equally well fabricated in a p-inverted channel regime, or for either the n- or p-type accumulation regime but, however, for the depletion type of realization, the resistance per unit length would be non-uniform and analysis would be more complicated, similarily with the junction field effect transistor.

This thesis takes elements from network analysis to predict the characteristics of a Kaufman type filter in Chapter I, then takes MOS-FET carrier relations from the literature, to design the filter in Chapter II. On design completion, a computed network solution is presented to demonstrate realizability of the characteristics also in Chapter II, and finally, the actual filter is fabricated in the laboratory and it is analyzed. The emphasis of this thesis is, however, to describe the experimental processes used in fabricating the device and the conclusions will be on the actual devices produced.

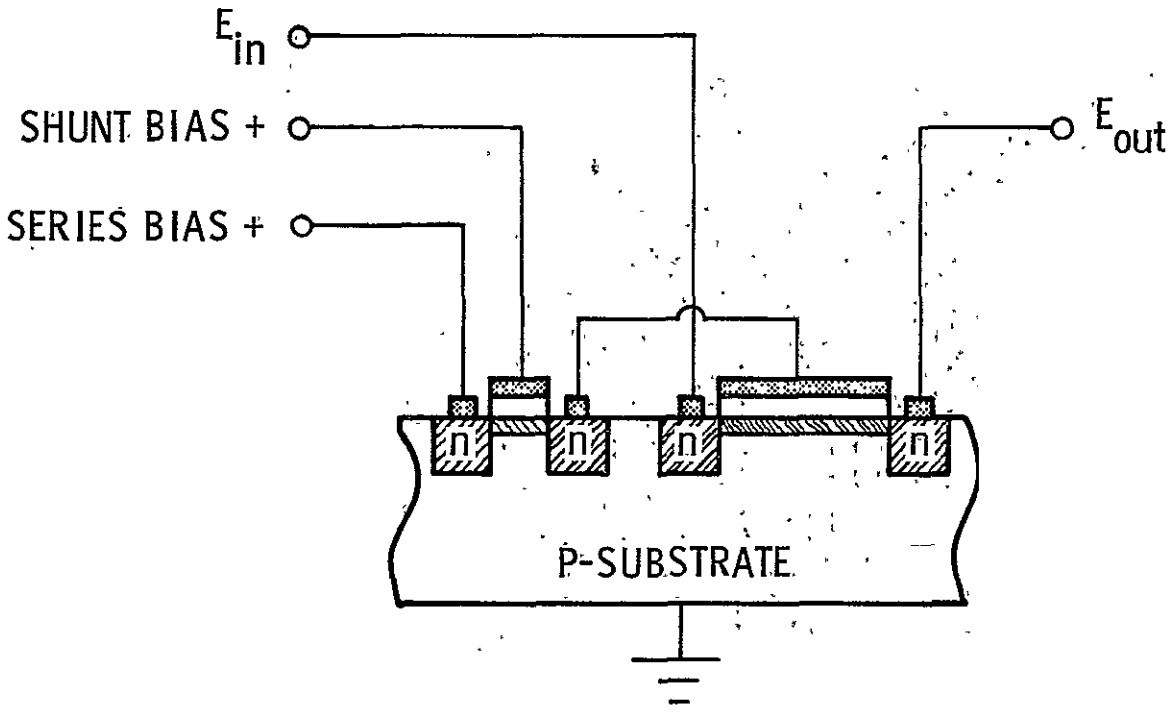


Figure 2.- Diagram of the proposed network.

Theoretical Preliminaries

The equations for Kaufman's "novel" null may be derived by starting with the impedance matrix of a uniform distributed network or transmission line

$$Z = Z_o \begin{bmatrix} \coth \Gamma d & \operatorname{csch} \Gamma d \\ \operatorname{csch} \Gamma d & \coth \Gamma d \end{bmatrix} \tag{1}$$

with the characteristic impedance of the line Z_o and the transmission coefficient Γ and a line whose length is 'd.

For the uniformily distributed R-C case (URC):

$$z_o = \sqrt{\frac{r_o}{sc_o}}$$

$$\Gamma = \sqrt{sr_oc_o}$$

where r_o and c_o are, respectively, the resistance and capacitance per unit length on the line. Then

$$Z_{URC} = \sqrt{\frac{r_o}{sc_o}} \begin{bmatrix} \coth d\sqrt{sr_oc_o} & \operatorname{csch} d\sqrt{sr_oc_o} \\ \operatorname{csch} d\sqrt{sr_oc_o} & \coth d\sqrt{sr_oc_o} \end{bmatrix} \tag{2}$$

or

$$Z_{URC} = \begin{bmatrix} \sqrt{\frac{r_o}{sc_o}} \coth d\sqrt{sr_oc_o} & \sqrt{\frac{r_o}{sc_o}} \operatorname{csch} d\sqrt{sr_oc_o} \\ \sqrt{\frac{r_o}{sc_o}} \operatorname{csch} d\sqrt{sr_oc_o} & \sqrt{\frac{r_o}{sc_o}} \coth d\sqrt{sr_oc_o} \end{bmatrix} \tag{3}$$

or for simplicity

$$Z_{URC} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \tag{4}$$

The network has been represented as an equivalent tee in Figure 3(a). The variables in Figure 3 are:

$$Z_1 = Z_{11} - Z_{12}$$

$$Z_2 = Z_{22} - Z_{21}$$

and

$$Z_3 = Z_{21}.$$

But since the network is uniform and symmetrical, then it is bilateral and therefore both $Z_{11} = Z_{22}$ and $Z_{12} = Z_{21}$. In single subscripted notation this is:

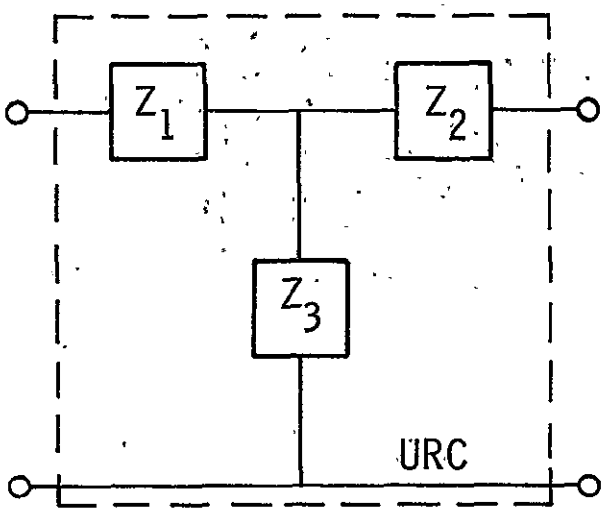
$$Z_1 = Z_{11} - Z_{12}$$

$$Z_2 = Z_1$$

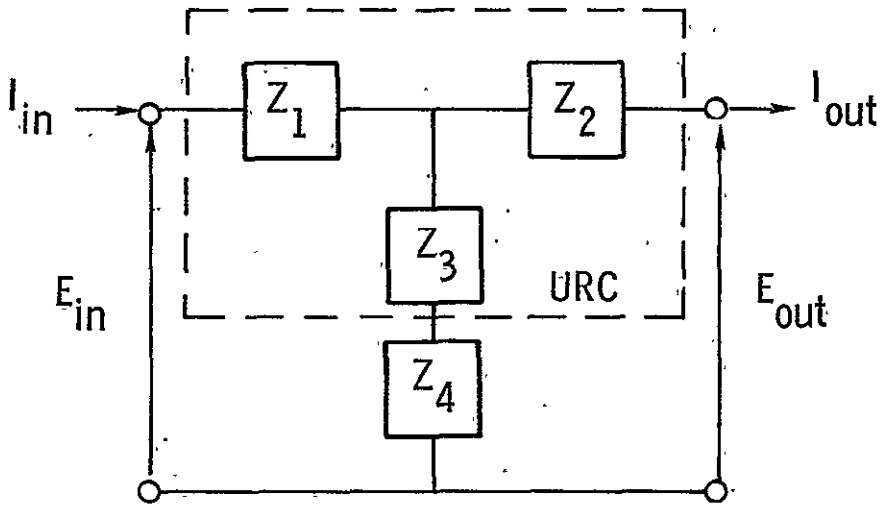
$$Z_3 = Z_{12}.$$

If now, one additional impedance is added into the branch containing Z_3 of the tee equivalent, the new network may be given unique features. Redrawing the tee now in Figure 3(b) and calling the new impedance Z_4.

For later discussion Z_1 and Z_2 may be described as Z_{series} and the combination of Z_3 and Z_4 may be described as Z_{shunt}.



(a) Tee representation of URC.



(b) URC tee with additional impedance Z_4.

Figure 3.- Tee representations of the uniformly distributed RC network.

It is now expedient to write the open circuit transfer function for this network. From Figure 3(b)

$$E_{in} = I_{in} (Z_1 + Z_3 + Z_4)$$

$$E_{out} = I_{in} (Z_3 + Z_4)$$

$$H(s) = \frac{E_{out}}{E_{in}} = \frac{Z_3 + Z_4}{Z_1 + Z_3 + Z_4} \tag{5}$$

In terms of the two subscripted notation equation (5) becomes:

$$H(s) = \frac{Z_4 + Z_{12}}{Z_4 + Z_{11}} \tag{6}$$

or equivalently

$$H(s) = \frac{Z_4 + \sqrt{\frac{r_o}{sc_o}} \operatorname{csch} \left(d \sqrt{sr_o c_o}\right)}{Z_4 + \sqrt{\frac{r_o}{sc_o}} \coth \left(d \sqrt{sr_o c_o}\right)} \tag{7}$$

Assume Z_4 is resistive only and has a value R_x.

$$H(s) = \frac{R_x + \sqrt{\frac{r_o}{sc_o}} \operatorname{csch} \left(d \sqrt{sr_o c_o}\right)}{R_x + \sqrt{\frac{r_o}{sc_o}} \coth \left(d \sqrt{sr_o c_o}\right)} \tag{8}$$

$$H(s) = \frac{R_x \sinh\left(d\sqrt{sr_oc_o}\right) + \sqrt{\frac{r_o}{sc_o}}}{R_x \sinh\left(d\sqrt{sr_oc_o}\right) + \sqrt{\frac{r_o}{sc_o}} \cosh\left(d\sqrt{sr_oc_o}\right)} \tag{9}$$

It is convenient to simplify the analysis by changing notation to Kaufman's notation. Let:

$$\omega_1 = \frac{2}{r_o c_o d^2} \qquad \text{(A fixed frequency)}$$

$$\gamma = \frac{\omega}{\omega_1}^{1/2} \qquad \text{(A frequency variable)}$$

$$\alpha = \frac{r_o d}{R_x} \qquad \text{(A pure number)}$$

$$\mu(\omega) = (1 + j)\gamma = (1 + j)\left(\frac{\omega}{\omega_1}\right)^{1/2} \qquad \text{(A complex frequency variable)}$$

Substituting these variables one by one in the H(s) above gives sequentially

$$H(s) = \frac{\frac{r_o d}{R_x} + \sqrt{\frac{2s}{\omega_1}} \sinh\left(\sqrt{\frac{2s}{\omega_1}}\right)}{\frac{r_o d}{R_x} \cosh\left(\sqrt{\frac{2s}{\omega_1}}\right) + \sqrt{\frac{2s}{\omega_1}} \sinh\left(\sqrt{\frac{2s}{\omega_1}}\right)} \tag{10}$$

$$H(s) = \frac{\alpha + \sqrt{\frac{2s}{\omega_1}} \sinh\left(\sqrt{\frac{2s}{\omega_1}}\right)}{\cosh\left(\sqrt{\frac{2s}{\omega_1}}\right) + \sqrt{\frac{2s}{\omega_1}} \sinh\left(\sqrt{\frac{2s}{\omega_1}}\right)} \tag{11}$$

$$H(j\omega) = \frac{\alpha + \mu \sinh \mu}{\cosh \mu + \mu \sinh \mu} \tag{12}$$

This is Kaufman's equation in his original notation.

Setting the numerator equal to zero gives

$$0 = \alpha + \mu \sinh (\mu) \tag{13}$$

Substituting in terms of complex frequency variables to find solutions gives

$$0 = \alpha + \left[(1 + j)\gamma\right] \sinh \left[(1 + j)\gamma\right] \tag{14}$$

or expanding once in terms of the real frequency variable γ gives

$$0 = \alpha + (\gamma + j\gamma)(\sinh \gamma \cdot \cosh j\gamma + \cosh \gamma \cdot \sinh j\gamma) \tag{15}$$

or

$$0 = \alpha + (\gamma + j\gamma)(\sinh \gamma \cdot \cos \gamma + \cosh \gamma \cdot j \sin \gamma) \tag{16}$$

and expanding still further gives

$$0 = \alpha + \gamma \sinh \gamma \cos \gamma - \gamma \cosh \gamma \sin \gamma + j\gamma \cosh \gamma \sin \gamma + j\gamma \sinh \gamma \cos \gamma \tag{17}$$

If one separates the real and imaginary parts and then solves for the imaginary part of equation (17) one gets:

$$\cosh \gamma \sin \gamma = -\sinh \gamma \cos \gamma \tag{18a}$$

or

$$\tan \gamma = -\tanh \gamma \tag{19a}$$

Similarly for the real part one gets:

$$\alpha = \gamma \cosh \gamma \sin \gamma - \gamma \cos \gamma \sinh \gamma \qquad (18b)$$

From solving equation (19a) numerically on a HP 9100A desk calculator one gets the following γ's.

$$\gamma_1 = 2.3650$$

$$\gamma_2 = 4.7124$$

$$\gamma_3 = 5.4978$$

$$\gamma_4 = 7.8540$$

which differ significantly from Kaufman's solutions in the third decimal place.

From equation (18b), corresponding to these γ's are the following α's:

$$\alpha_1 = 17.7985$$

$$\alpha_2 = -262.308$$

$$\alpha_3 = -949.162$$

$$\alpha_4 = 10115.81.$$

The denominator of $H(j\omega)$ has the equation

$$D(j\omega) = \alpha \cosh \mu + \mu \sinh \mu. \qquad (20)$$

Expanding this denominator function for evaluation gives:

$$D(j\gamma) = \alpha \cosh(\gamma + j\gamma) + (\gamma + j\gamma) \sinh (\gamma + j\gamma) \qquad (21)$$

$$D(j\gamma) = (\alpha)(\cosh \gamma \cdot \cosh j\gamma + \sinh \gamma \cdot \sinh j\gamma)$$
$$+ (\gamma + j\gamma)(\sinh \gamma \cdot \cosh j\gamma + \cosh \gamma \cdot \sinh j\gamma) \qquad (22)$$

$$D(j\gamma) = \alpha \cosh \gamma \cos \gamma + \alpha j \sinh \gamma \sin \gamma + \gamma \sinh \gamma \cos \gamma$$
$$- \gamma \cosh \gamma \sin \gamma + j\gamma \cosh \gamma \sin \gamma + j\gamma \sinh \gamma \cos \gamma \quad (23)$$

Separating into real and imaginary parts, one gets:

$$\text{Re } D(j\gamma) = \alpha \cosh \gamma \cos \gamma + \gamma \sinh \gamma \cos \gamma - \gamma \cosh \gamma \sin \gamma \quad (24a)$$

$$\text{Im } D(j\gamma) = \alpha \sinh \gamma \sin \gamma + \gamma \cosh \gamma \sin \gamma + \gamma \sinh \gamma \cos \gamma \quad (24b)$$

Now substituting in α_1, γ_1 gives:

$$\text{Re } D(j\gamma_1) = -85.9655 \quad (25a)$$

$$\text{Im } D(j\gamma_1) = +65.8017 \quad (25b)$$

It can be seen then that if a network can be designed such that

$$\alpha_1 = 17.7985$$

with a

$$\gamma_1 = 2.3650$$

or

$$\gamma_1^2 = 5.5932$$

then

$$\omega_{null} = 5.5932 \omega_1$$

or in the original notation:

$$\omega_{null} = 5.5932\, \omega_1 = \frac{2(5.5932)}{(r_o d)(c_o d)} \quad (26)$$

and

$$\frac{r_o d}{R_x} = 17.7985 \tag{27}$$

If equations (26) and (27) are used in designing a semiconductor network, and if such relations are practical to implement, the network will have the "notch" effects described by Kaufman.

CHAPTER II

DESIGN AND SIMULATION

Design

A Kaufman type "novel" null network is a reasonable extension of the traditional Metal Oxide Silicon Field Effect Transistor (MOS-FET), and the MOS-FET offers a logical solution for some of the tunability problems of the null network.

Because of the bias versus channel resistivity relationship of the MOS-FET, it is possible to vary the equivalent surface resistance of the channel electrically (or optically or thermally). Advantage may be taken from this relationship if adequate geometries and bias operating points may be found. This chapter will examine these aspects of the problem.

If in equation (27), $\left(\frac{r_o d}{R_x}\right)$ can be constrained to be the constant 17.7985 while the absolute magnitudes of $r_o d$ and R_x are somehow adjustable electrically with $c_o d$ considered to be fixed, then the frequency ω_{null} will vary with $\frac{1}{r_o d}$.

If one starts with a relationship for a generalized resistance, $\mathcal{R}$, as a function of a bulk resistivity, ρ, and dimensions, l, a length, and A, surface area normal to a current flow in a resistive material. Now let l be identically equal to d and A be identically equal to the product of a thickness, t, and the width, w, already discussed.

$$\mathcal{R} = \frac{\rho l}{A} = \frac{\rho d}{tw}$$

In particular

$$\mathcal{R} = \left(\frac{\rho}{t}\right)\left(\frac{d}{w}\right)$$

let ρ and t be electrically variable as a pair and d and w be fixed by the geometry and the process. Let $\left(\rho/t\right)$ also be described by ρ_s, a surface resistivity with dimensions of ohms per square.

Re-examining equation(27),

$$17.7985 = \frac{r_o d}{R_x}$$

if now both the distributed resistor $r_o d$ and the shunting resistor R_x are fabricated on the same substrate by the same techniques and are biased appropriately, then their ρ_s will be the same.

Therefore,

$$17.7985 = \frac{\left(\frac{\rho}{t}\right)\left(\frac{d}{w}\right)}{\left(\frac{\rho}{t}\right)\left(\frac{D}{W}\right)} \tag{28}$$

or $\left(\frac{\rho}{t}\right)$ may be removed from the problem and this problem now results in one of geometry and bias only.

$$17.7985 = \frac{\frac{d}{w}}{\frac{D}{W}} \tag{29}$$

If for convenience $\frac{D}{W}$ is chosen equal to 1, then

$$\frac{d}{w} = 17.7985 \tag{30}$$

There are three implicit problems in this simplification. The first problem is that for $\left(\frac{\rho}{t}\right)$ to be the same constant for both devices

they must be biased to the same potential with respect to their own channels. This requires two separate biasing networks in the physical circuit.

The second problem is that to this point all capacitive effects have been ignored for Z_4, that is R_x was assumed to be equal to Z_4. Since R_x is essentially a MOS-FET, the channel resistance is varied essentially by a capacitive effect, but it is desirable to minimize the capacitance. For this purpose $\frac{D}{W}$ was chosen equal to 1, since for a minimal rectangular geometry, this is a convenient shape. This problem is difficult to analyze in closed form so a computed solution will be used to determine to what extent the small capacitance is negligible.

The third problem is the maintenance of a constant capacitance through the "tuning range". That is over the range of $\left(\frac{\rho}{t}\right)$ values ($c_o d$) must be either ideally constant or at least predictable, in which case the bias versus null dependence will become complicated. This problem may also be sidestepped by a judicious choice of MOS type. At frequencies above 10 Khz for an "inverted" channel, the capacitance is constant over a wide range of bias values. Then the devices chosen to implement this filter type are essentially one large area inverted MOS-FET whose length is 17.7985 times the width, and one small square MOS-FET with minimal surface area, both on the same substrate, and both therefore processed together.

A good nominal frequency for design of such a pair is 100 Khz, since it is a frequency commonly used in voltage controlled oscillators, which is one general area where this type of device offers unique

application. It is expected to be tunable over a wide range of frequencies from approximately 10 Khz to perhaps 5 Mhz, the useful range of this type of MOS-FET.

If now, 100 Khz is chosen as the design frequency with the bias voltages of each of the gates with respect to their substrate (V_G) while referenced to the turn-on voltage (V_T) of the invividual MOS-FET being ($V_G - V_T$); and additionally, both being chosen as 1.64 volts nominally, such a device pair may be designed.

For this particular construction, 1 ohm centimeter p-type material was chosen for the host substrate for two reasons, convenience and accessibility. For this resistivity

$$N_A \sim 1.45 \times 10^{16}/cm^3$$

and

$$\mu_n = 10^3 cm^2/V\text{-sec.}$$

but this is for the bulk. For a thin film however,[8] $\mu_n \sim 500\ cm^2/V\text{-sec.}$

Since f_{null} is chosen to be 100 Khz,

$$\omega_{null} = 5.5932\ \omega_1 \qquad \text{(from equation (26))}$$

then $\omega_1 = 112{,}336$

or since

$$\omega_1 = \frac{2}{r_o c_o d^2} \tag{31}$$

then

$$r_o c_o d^2 = 1.78037 \times 10^{-5} \tag{32}$$

If an inverted channel is used as the distributed element and the frequencies are greater than or equal to 10 Khz, the capacitance between gate and channel and channel and ground may be represented as the two capacitors C_{GC} and C_{CS} as shown in Figure 4.

There are two capacitors for this circuit biasing regime: C_{GC} is the capacitance between the gate and channel due to the oxide alone and C_{CS} is the capacitance between the channel and the substrate due to the depletion region between the channel and the substrate.

Looking at these capacitances in more general form where $\mathcal{C}$ is a generalized capacitance, ϵ_o is the permitivity of free space, ϵ is the relative permitivity of dielectric, A is the surface area of the capacitor and t is the dielectric thickness.

$$\mathcal{C} = \frac{\epsilon\epsilon_o A}{t}$$

Calculating C_{CS} first with $\epsilon_{silicon}$ reported in Grove[9] equal to 11.7 and assuming that the depletion layer thickness for the substrate material is approximately 0.5μ as reported in Grove[10] then,

$$C_{CS} = \frac{(11.7)(8.854 \times 10^{-12}) \times 10^{-2}}{(5 \times 10^{-7})(10^{2})} \text{ f/cm}^2$$

$$C_{CS} = 2.0718 \times 10^{4} \text{ pf/cm}^2 \qquad (33)$$

If the gate to channel dielectric is chosen to be 3000Å of thermally grown SiO_2 with a permitivity reported by Grove[9] to be:

$$\epsilon_{SiO_2} = 3.4$$

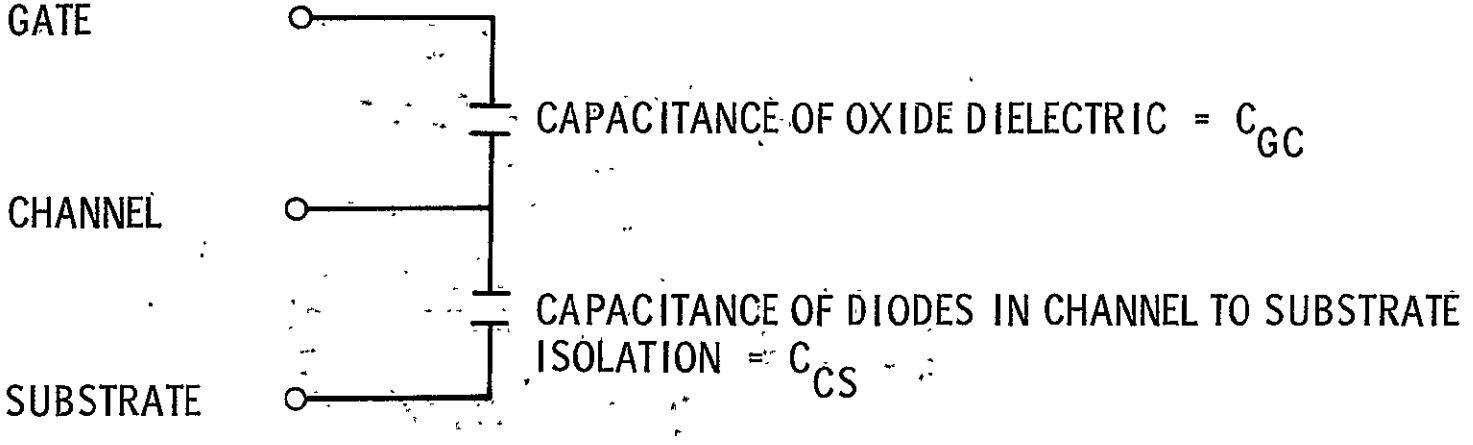


Figure 4.- Equivalent inverted channel capacitances.

then

$$C_{GC} = \frac{(3.4)(8.854 \times 10^{-12}) \times 10^{-2}}{3(10^{3})(10^{-8})}$$

or

$$C_{GC} = 1.00345 \times 10^{4} \quad pf/cm^{2} \tag{34}$$

then finally,

$$c_{o} = 1.00345 \times 10^{4} \text{ w pf/cm.} \tag{35}$$

Now C_{GC} represents the desired capacitance in the novel null device and C_{CS} represents a parasitic capacitance between the channel of the device and ground. This effective shunting capacitance may have three effects on the device, first it may lower the 'Q' of the null device, secondly, it may shift the null frequency slightly from the predicted value, and thirdly it may cause attenuation over all the range of the null, but will be more pronounced at the higher frequencies. C_{GS} is ignored here but will be treated in this analysis as a parasitic in the numerical analysis, since it does not enter directly into the null effect.

Since by equation (29)

$$r_{o}c_{o}d^{2} = RC = 1.78037 \times 10^{-5}$$

it is now possible to get an approximation for an adequate value of d. Since for an inversion n-channel MOS-FET the channel conductance, g, is given by [11]

$$g = \frac{w}{d}(\mu_n)C_{ox}(V_G - V_T) \tag{36}$$

where μ_n is the electron mobility; C_{ox} is the gate to channel capacitance and $(V_G - V_T)$ is the bias voltage referenced to V_T, the turn on voltage for the device.

The channel resistance is then R, the reciprocal of g, or

$$R = \frac{d}{w}\left(\frac{1}{\mu_n}\right)\left(\frac{1}{C_{ox}}\right)\left(\frac{1}{V_G - V_T}\right) \tag{37}$$

and the channel capacitance is then

$$C = C_{ox}\, wd \tag{38}$$

Substituting these relations into equation (29) gives

$$1.78037 \times 10^{-5} = \left(\frac{d}{w}\right)\left(\frac{1}{\mu_n}\right)\left(\frac{1}{C_{ox}}\right)\left(\frac{1}{V_G - V_T}\right)(C_{ox})(wd) \tag{39}$$

Simplifying this gives

$$d^2 = \mu_n(V_G - V_T)(1.78037 \times 10^{-5}) \tag{40a}$$

$$d^2 = (V_G - V_T)(8.90185 \times 10^{-3}) \tag{40b}$$

For

$$(V_G - V_T) = 1.64 \text{ V.} \tag{41}$$

which is a reasonable bias voltage,

$$d = 0.121 \text{ cm.} = 0.05084 \text{ inches,} \tag{42}$$

then equation (30) requires

$$w = 0.006798 \text{ cm.} = 0.00268 \text{ inches} \tag{43}$$

For a minimal geometry configuration it is convenient to let

$$D = 0.5 \text{ mil} = 1.27 \times 10^{-3} \text{ cm.} \tag{44}$$

and, therefore,

$$W = 0.5 \text{ mil} = 1.27 \times 10^{-3} \text{ cm.} \tag{45}$$

It is now reasonable to compute the total channel resistance and capacitance for both the series and the shunting MOS-FET's, for a bias voltage $(V_G - V_T)$ equal to 1.64 V. By equation (37)

$$R = \left(\frac{d}{w}\right)\left(\frac{1}{\mu_n}\right)\left(\frac{1}{C_{ox}}\right)\left(\frac{1}{V_G - V_T}\right)$$

$$R = 2.163 \text{ M}\Omega \tag{46}$$

and by equation (38)

$$C = C_{ox}(wd)$$

$$C = 8.232 \text{ pf.} \tag{47}$$

Similarly for the shunt device

$$R_s = 0.1215\ M\Omega \tag{48}$$

$$C_s = 1.618 \times 10^{-6}\ pf. \tag{49}$$

The tunability curve of this network is expected to vary with voltage as does r_o. That is, from equations (26) and (31),

$$\omega_{null} = 5.5932 \left(\frac{2}{r_o c_o d^2}\right) \tag{50}$$

but with c_o and d considered to be fixed, then ω_{null} varies with the reciprocal of r_o. But it must be noted from equation (37) that

$$r_o = \left(\frac{1}{w}\right)\left(\frac{}{\mu_n}\right)\left(\frac{1}{C_{ox}}\right)\left(\frac{1}{V_G - V_T}\right) \tag{51}$$

then since ω_{null} varies reciprocally with r_o and since r_o varies reciprocally with the bias voltage $(V_G - V_T)$, then the frequency ω_{null} varies directly with voltage.

As a matter of fact, in general

$$\omega_{null} = (5.5932)(2)\left(\frac{1}{w}\right)\left(\frac{1}{\mu_n}\right)\left(\frac{1}{C_{ox}}\right)\left(\frac{1}{V_G - V_T}\right)(C_{ox})(w)\ d^2 \tag{52}$$

or

$$\omega_{null} = \frac{(2)(5.5932)\mu_n'(V_G - V_T)}{d^2} \tag{53}$$

This is the tunability relationship which is valid for any substrate or any bias provided the network is designed to make parasitics negligible.

Simulation

In this section, two distinct networks are discussed, both being approximations to the null network. Each network will be approximated for solution on DLANET, a digital computer program which solves the transfer functions of networks composed of three terminal distributed R-C devices. This program is officially entitled "DLANET - A Digital Computer Program for the Analysis of Distributed, Lumped, Active Networks" and was written by L. P. Huelsman[12] at the University of Arizona. This program was adapted to be compatible with the CDC 6600 computer which is available and this program was used to prepare the results discussed in this chapter.

First, frequency response of the transfer function of the idealized network will be discussed. Then the frequency response of the transfer function of the idealized network with both the parasitic and actual measurement loading conditions expected will be discussed.

The idealized network with its values described previously in equations (46) - (49):

$$\left.\begin{aligned} R_{series} &= 2.163\ M\Omega \\ C_{series} &= 8.232\ pf \end{aligned}\right\} (V_A - V_T) = 1.64\ V.$$

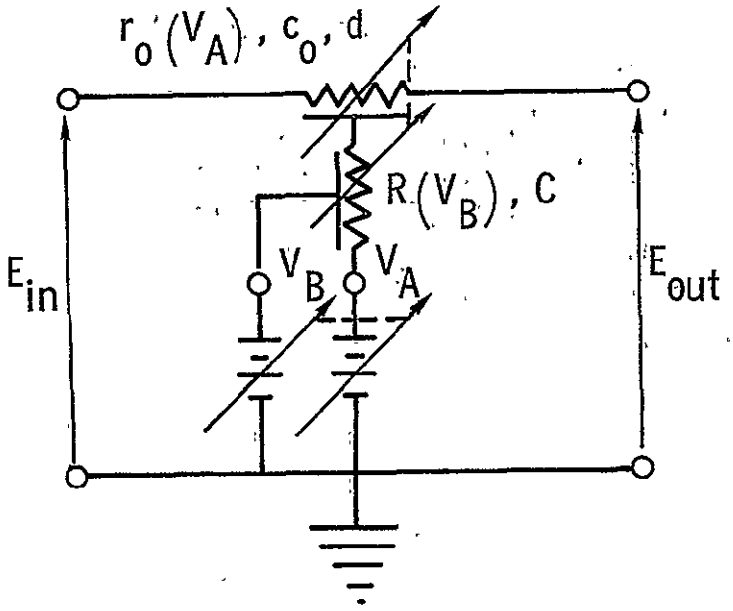
$$\left.\begin{aligned} R_{shunt} &= 0.1215\ M\Omega \\ C_{shunt} &= 1.618 \times 10^{-6}\ pf \end{aligned}\right\} (V_B - V_T) = 1.64\ V.$$

is redrawn together with its bias supplies as Figure 5(a) with V_T the turn on voltage for each device and V_A and V_B the bias voltages. For the sake of compatibility with DLANET, a unity gain, voltage controlled voltage source is added to the network in Figure 5(b). The network of Figure 5(b) is amenable then to direct solution on a digital computer by use of DLANET.

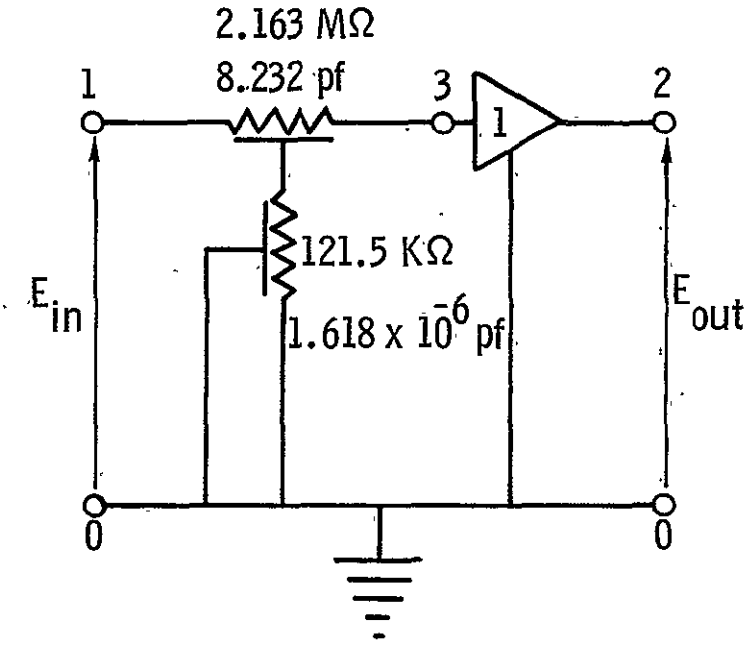
The proposed network has been solved for numerical results on DLANET. The plotted computer results are presented as Figure 6. The network is essentially solved by a lumped element approach, and the distributed element is approximated by up to fifty "L" sections. Both distributed devices have been approximated here by fifty "L" sections. Examining five possible network bias points with $V_A = V_B$ gives the five values in Table I.

TABLE I

Plotted point	Bias voltage	Calculated circuit values	Predicted null frequencies
A)	$(V_A - V_T) = 0.164$ V	$R_{series} = 2163$ MΩ $R_{shunt} = 1.215$ MΩ	$f_{null} = 10$ Khz
B)	$(V_A - V_T) = 0.82$ V	$R_{series} = 4.326$ MΩ $R_{shunt} = 0.2430$ MΩ	$f_{null} = 50$ Khz
C)	$(V_A - V_T) = 1.64$ V	$R_{series} = 2.163$ MΩ $R_{shunt} = 0.0215$ MΩ	$f_{null} = 100$ Khz
D)	$(V_A - V_T) = 3.28$ V	$R_{series} = 1.082$ MΩ $R_{shunt} = 0.0608$ MΩ	$f_{null} = 200$ Khz
E)	$(V_A - V_T) = 16.4$ V	$R_{series} = 0.2163$ MΩ $R_{shunt} = 0.01215$ MΩ	$f_{null} = 1$ Mhz



(a) Null network with bias supplies.



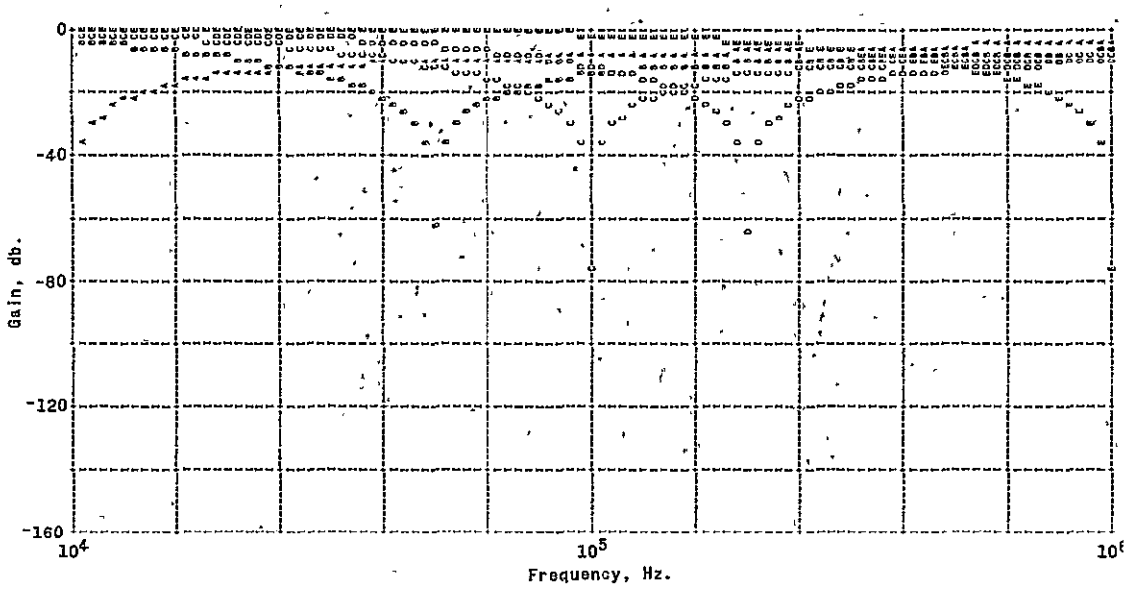
(b) Null network with element values and VCVS.

Figure 5.- Proposed null network for simulation.

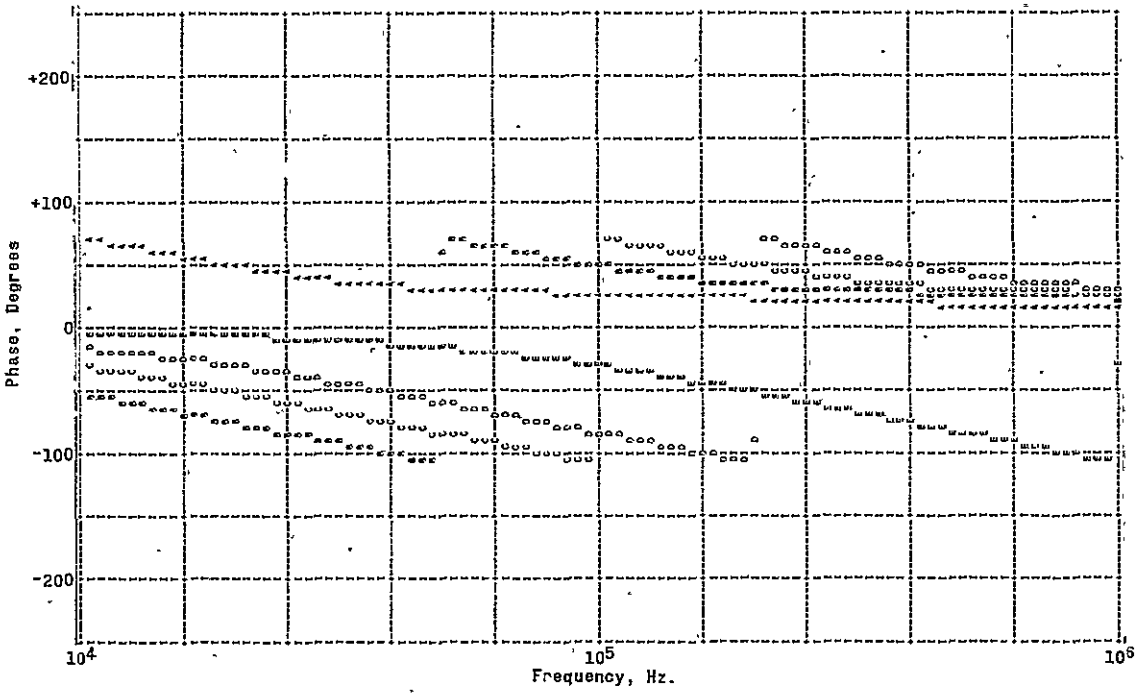
These predicted results are verified and plotted by the computer analysis. The frequency response of the transfer function is plotted both in magnitude and phase in logarithmic frequency increments in two parts. In Figure 6(a) the gain in db is plotted as a logarithmic function of frequency. This plot has 50 points per decade over the range of 10 Khz to 1 Mhz. In Figure 6(b) the phase in degrees is plotted as a logarithmic function of frequency. This plot also has 50 points per decade over the same range. The actual program is listed as Appendix A of this thesis, and tabulated computer output for points plotted as C in Figure 6(a) and 6(b) is included as Appendix B. Figure 6 demonstrates the tunability relationship as derived in equation (53), and demonstrates that, within the simplifications stated, the predicted results are reasonable.

Now, the network may be reevaluated in a form expected for actual measurement with the actual parasitics and loadings imposed by the measurement circuitry.

First, the voltmeter used to measure the output has an input impedance of 10 megohms shunted by 25 picofarads, and secondly, the capacitance to substrate of the channel is approximately 17.04 picofarads and finally the series impedance of the voltage source may be assumed to be approximately 10 megohms. These test condition approximations are presented symbolically in Figure 7 and have been applied to the computer program and have been analyzed and plotted as Figure 8. Figure 8(a) is then the magnitude of the transfer function expected to be measured and Figure 8(b) is the phase. The actual computer data for



(a) Magnitude of transfer function versus frequency.



(b) Phase of transfer function versus frequency.

Figure 6.- Computed frequency response.

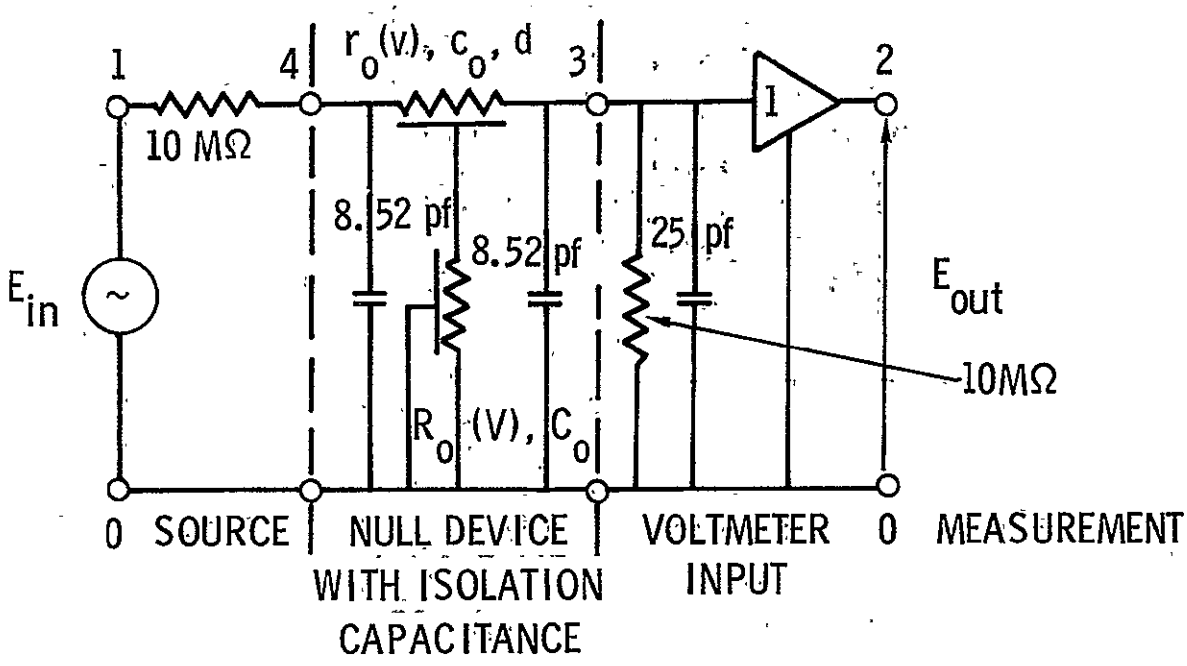
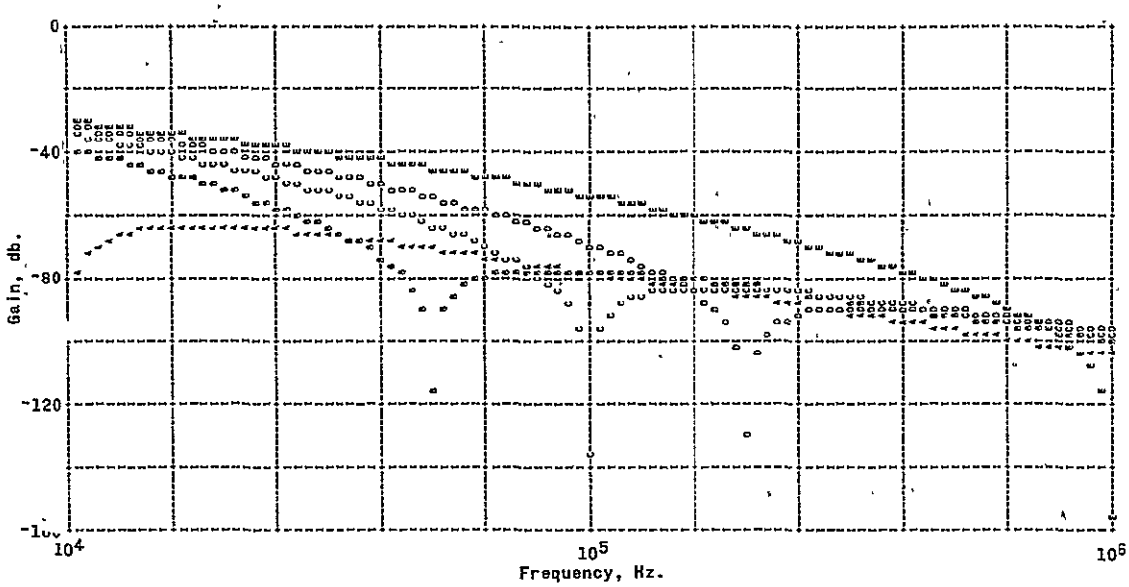
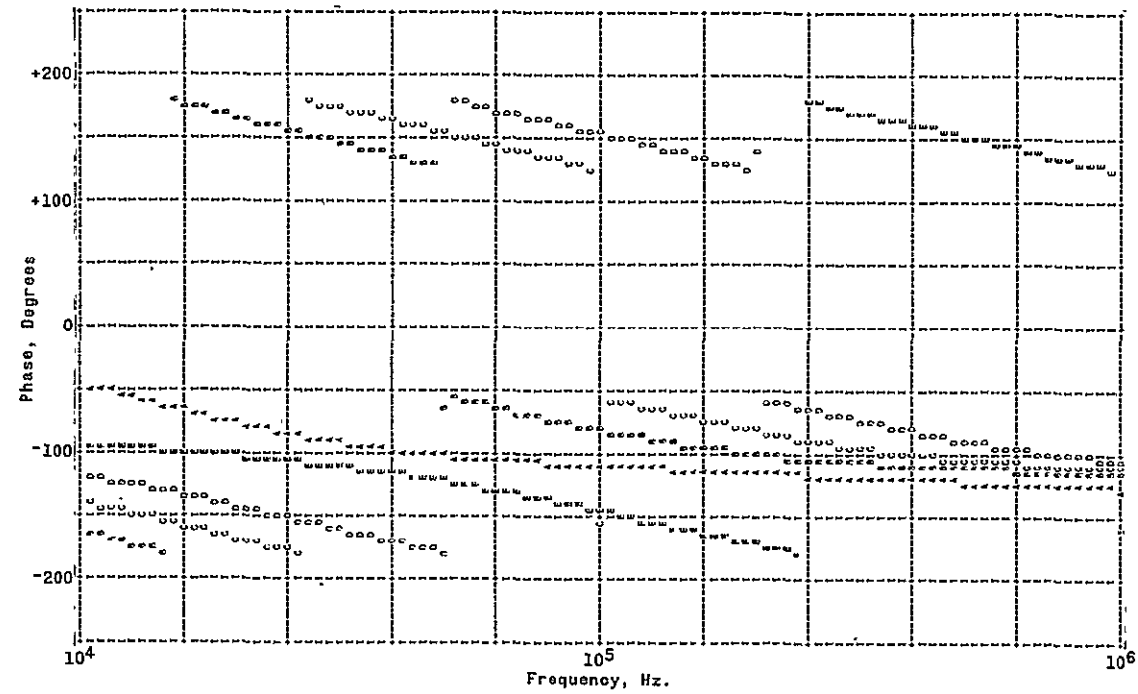


Figure 7.- Measurement condition simulation diagram.



(a) Magnitude of transfer function versus frequency.



(b) Phase of transfer function versus frequency.

Figure 8.- Measurement condition computed frequency response.

points plotted as C in Figure 8 is also included in Appendix B. From this it is clear that the device will have an upper useful limit in the low megahertz range because of both resistive and capacitive loading and substrate leakage. These results also indicate that if the device can be fabricated in the design configuration, it will behave as expected.

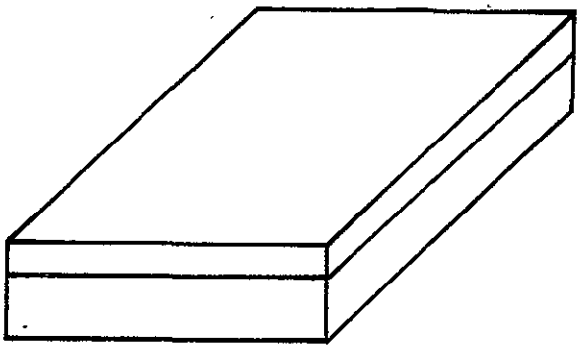
CHAPTER III

FABRICATION

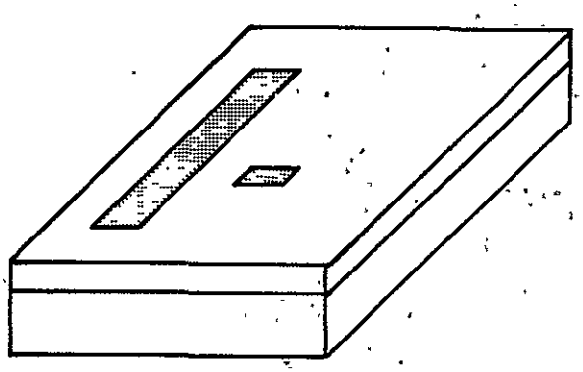
Test sample devices were fabricated to demonstrate the null effect. This chapter will discuss the actual procedures followed in preparing the devices for test.

The devices were prepared on 100 mil × 100 mil chips with approximately 32 expected devices per processed wafer. They were prepared by a typical overlay process, such as the one described by H. Bierman.[13] The fabrication steps for such a process are explained in detail in Figure 9. This fabrication regime is essentially an overlay masking process which is flexible in control, and is composed of 4 etches, one oxidation, and one source-drain diffusion.

Photo masks were designed, fabricated, photo reduced, and step and repeated, using the dimensions outlined in Chapter II. The oxidation and diffusion steps were planned to achieve the resulting device pair. Magnified photographs of each of the four final masks are included as Figure 10. An Aristo stabilene cutting table was used in the cutting of the original masks. A David W. Mann 1003 photo-reduction camera at a reduction of 10X was used to prepare step and repeat masters. A David W. Mann 992A master reticule alignment microscope was used to align the master plates for use in a David Mann Type 1080 step and repeat camera, set at a 10X reduction. The results were patterns of 100 mill square devices on a 2" × 2" Kodak high resolution plates which were used as masters. From these masters, contact prints were made

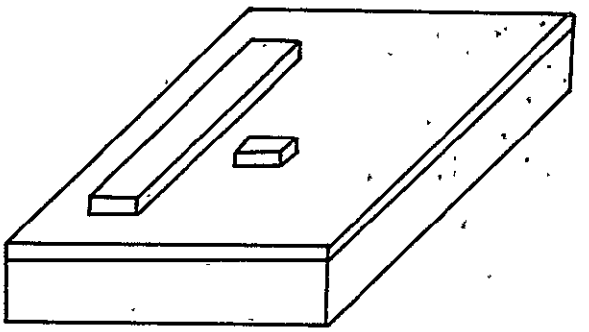


(a) P-TYPE HOST SUBSTRATE WITH 10,000 Å OF THERMALLY GROWN SiO_2

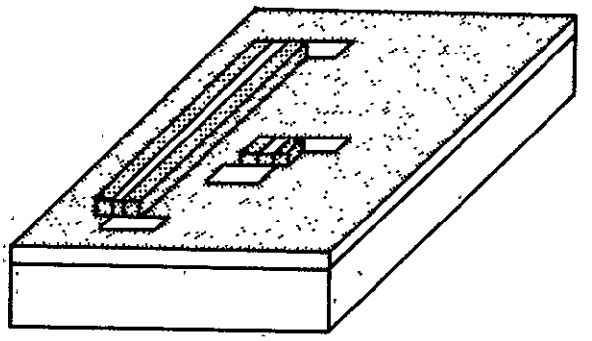


(b) PHOTO RESIST APPLIED EXPOSED, AND DEVELOPED; SUBSTRATE PREPARED FOR FIRST OXIDE ETCH; THIS ETCH DETERMINES GATE OXIDE THICKNESS AND LENGTH

Figure 9.- Typical MOS fabrication regime.

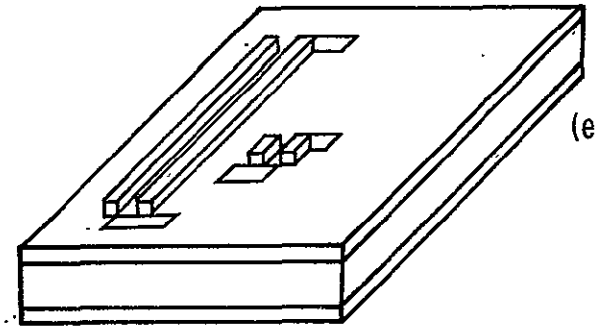


(c) CONCLUSION OF FIRST OXIDE ETCH; AREAS RAISED ARE 2000^{0}A HIGH; THIS HEIGHT DETERMINES FINAL GATE OXIDE THICKNESS AND LENGTH

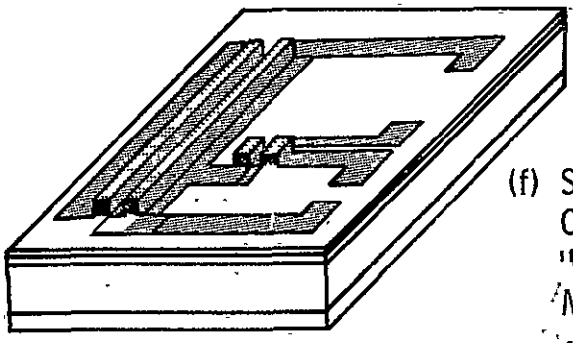


(d) PHOTO RESIST APPLIED, EXPOSED, AND DEVELOPED; SUBSTRATE PREPARED FOR SECOND OXIDE ETCH; THIS ETCH DETERMINES FINAL GATE OXIDE THICKNESS AND WIDTH AS WELL AS OPENS SUBSTRATE REGIONS FOR SOURCE-DRAIN DIFFUSIONS

Figure 9.- Continued.

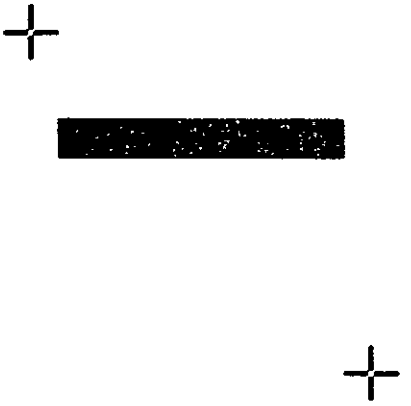


(e) CONCLUSION OF SECOND OXIDE ETCH; SOURCE-DRAIN DIFFUSION WINDOWS EXPOSED, CHANNEL LENGTHS AND WIDTHS FIXED, GATE OXIDE THICKNESS FIXED AT 2000^{o}A

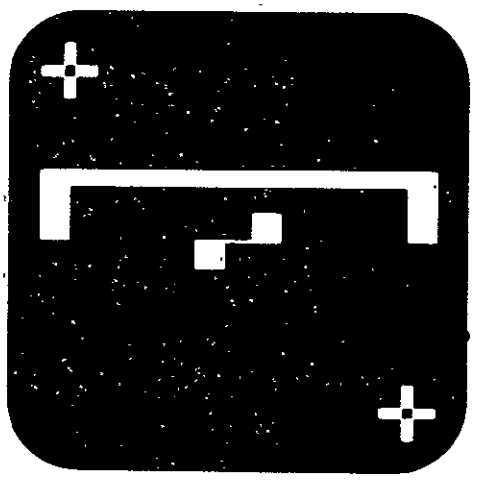


(f) SOURCE-DRAIN DIFFUSION COMPLETED; METALLIZATION "WINDOWS" PHOTO-RESISTED, MASKED, EXPOSED, DEVELOPED, AND ETCHED OF REGROWN OXIDE; ALUMINUM GATE AND INTER-CONNECTION METALLIZATION VACUUM DEPOSITED, PHOTO-RESISTED, MASKED, EXPOSED, DEVELOPED, AND ETCHED LEAVING COMPLETED CIRCUITS; PROCESSING REMAINING IS TO VACUUM DEPOSIT GOLD SUBSTRATE CONNECTION ON BACK, THEN SCRIBE AND BREAK WAFER.

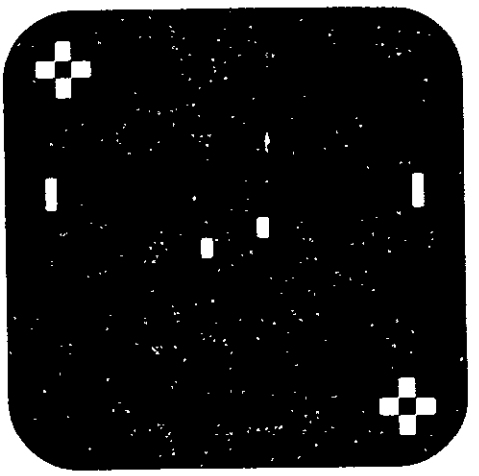
Figure 9.- Concluded.



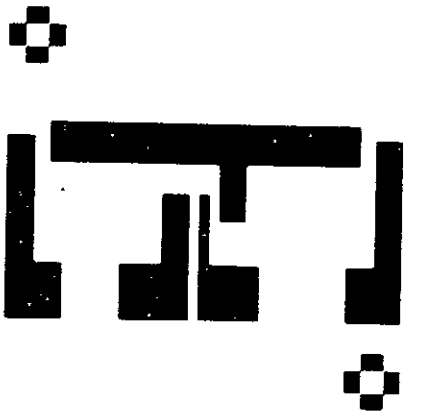
(a) First oxide mask.



(b) Second oxide mask (diffusion mask).



(c) Metallization contact window mask.



(d) Metallization mask.

Figure 10.- Four final masks.

also onto a 2" × 2" Kodak high resolution plates for subsequent production runs.

The wafers used were 1 ohm cm ± 10 per cent p-type and were supplied from Electronic Materials Inc. A copy of their boule evaluation report is included as Appendix C. The individual wafers were prepared for use by standard procedures referred to in the literature[14] and reproduced in Appendix D.

The first production lot consisted of twelve wafers. On these wafers the first oxide was grown in a standard oxidizing furnace shown in Figure 11. The furnace temperature was 1200° C ± 1° C. The water temperature was 75° C or a partial pressure of 289 torr, and the time for the actual oxidation was 190 minutes expecting to grown 10,000Å. The wafers were initially heated to furnace operating temperature in an oxidizing environment for minimal oxidation then the water vapor was put into the gas flow. At the conclusion of the oxidation the wafers were annealed for 30 minutes in dry nitrogen to remove dissolved water from the oxide.[15] The wafers were then coated with Shipley AZ-1350 photo-resist which was applied and used according to the manufacturer's instructions and briefly outlined in Appendix E.

The first etch was done using a calibrated etch to remove 2000Å of oxide referred to in Appendix F.[16] The second photo making step was followed as outlined in the process, and when the substrate was exposed in the desired diffusion areas, the etch was stopped quickly. The source-drain diffusion was carried out in a one step process in a Hevi-Duty furnace at a temperature of 1100° C for a 30 minute deposition

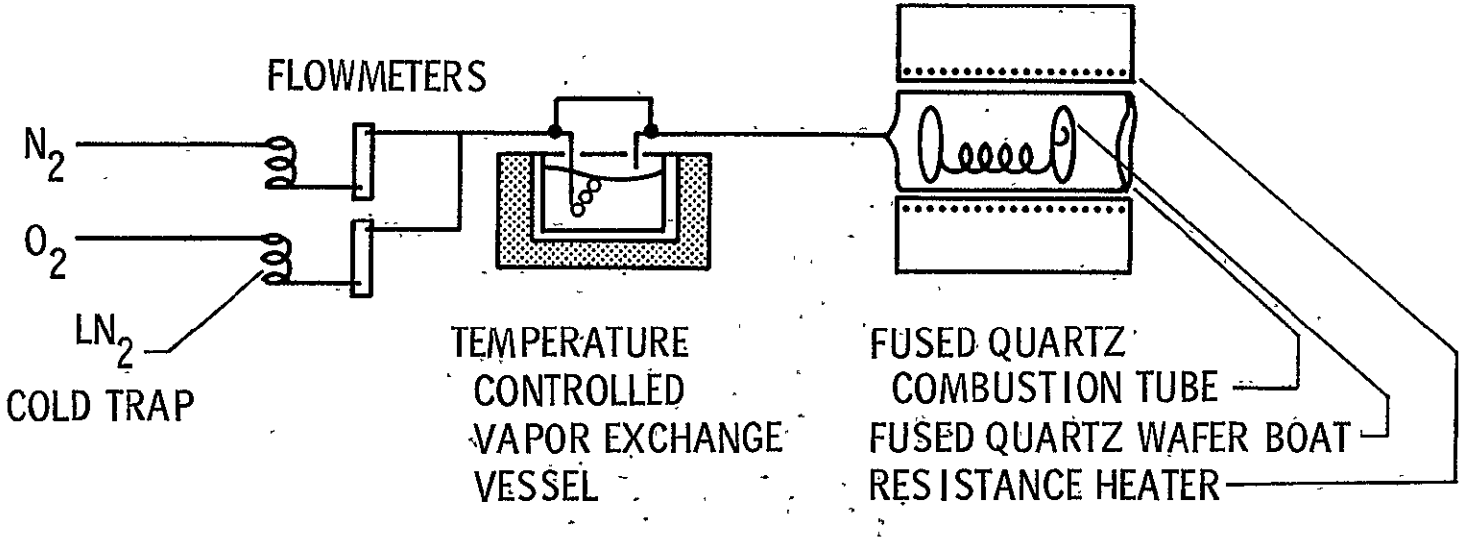


Figure 11.- Diagram of oxidation system.

step and no drive diffusion. The dopant in the gas flow was 50 parts per million of phosphine. The total flow was 1000 cc/min with 47 cc/min of O_2 flowing and the balance nitrogen. The P_2O_5 glass growth was expected to be approximately 1000Å. A picture of the diffusion furnace and the gas flow control panel are included as Figure 12. The metallization "windows" were then etched into the regrown oxide in the source drain regions, by use of the etch in Appendix F.

The aluminum metallization was applied by evaporation in a vacuum at a pressure of approximately 5×10^{-6} torr from a tungsten filament which had been cleaned according to procedures found in the literature[17] and outlined in Appendix D. The aluminum was heated to 250° C after evaporation for adherence purposes, then was photo masked and etched in an acidic aluminum etch whose composition is found in the literature[18] and as included in Appendix F. The aluminum was then simultaneously sintered to the silicon dioxide and alloyed with the silicon by heating to 460° C for 5 minutes in a vacuum of approximately 5×10^{-6} torr. The aluminum was sintered to the silicon dioxide for adherence and bonding purposes. It was alloyed with the silicon to form ohmic contacts with desired substrate areas. Finally gold was similarly vapor deposited on the back of the wafer and sequentially alloyed by heating for 2 minutes to 320° C. This was done to allow for substrate bonding and contacting. The contacts to the surface were checked for ohmic properties by evaporating a layer of the test metal over all the surface, then alloying it and then abrading it away through the center of the wafer and finally measuring a low resistance

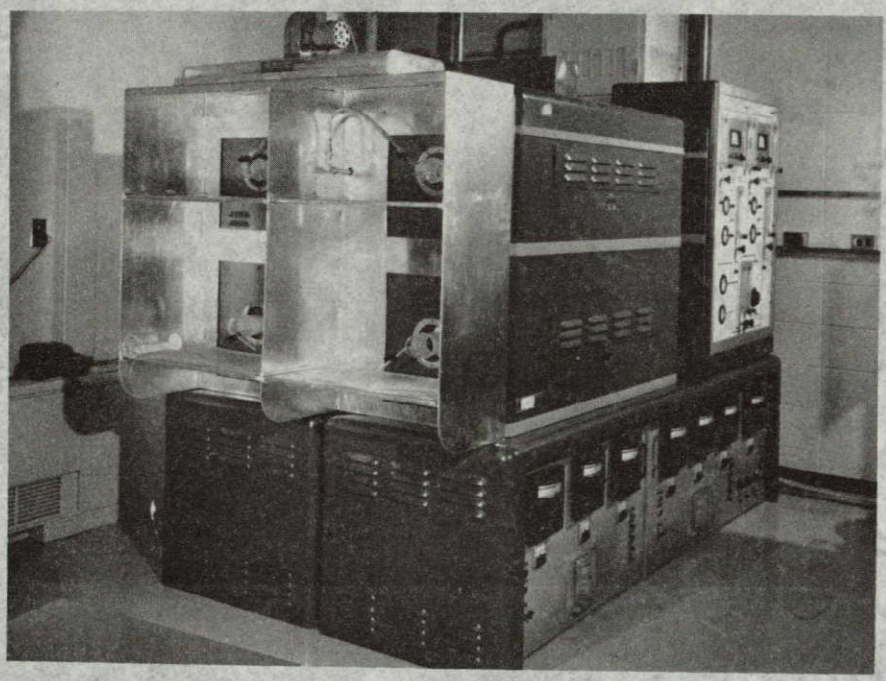


Figure 12.- Picture of diffusion furnace.

from side to side of the abraded area. A picture of one typical production wafer is included as Figure 13, and a circuit as Figure 14. The remaining eight wafers were then scribed and the dice separated. The scriber used was a Kulicke and Soffa manual type and the scribe pressure was 20 gm. The technique used was described in the literature,[19] and involved drawing the diamond stylus across the wafer in the proper crystalline direction as indicated in Figure 15. Six of the scribed wafers were broken along the scribe lines by rolling over the scribed wafer with a rubber printer's roller. The wafer was first placed scribed side down between two pieces of sheet plastic and then the sandwich was placed on a rubber pad which was softer than the roller, and the roller was passed over in both directions. The break was good and yielded approximately 25 devices per wafer out of approximately 30 possible. The devices were optically screened to cull out obvious defectives and about 80 devices remained.

The individual dice were to be put on headers made by Bendix Corp. and were called their "Square TO", a 12 pin, 1/2 in. × 1/2 in. header. Printed circuit boards were fabricated to hold the test headers so that flexible connections could be made to the individual pins of the header for testing.

Two devices were used per header for testing purposes. They were bonded to the header with Ohmex-Ag, a proprietary epoxy type material used for this purpose, which was cured at 200° C for 4 hours. Gold wires were then bonded to the contact pads to the terminal posts on the header. The bonds were of hot capillary thermocompression type,

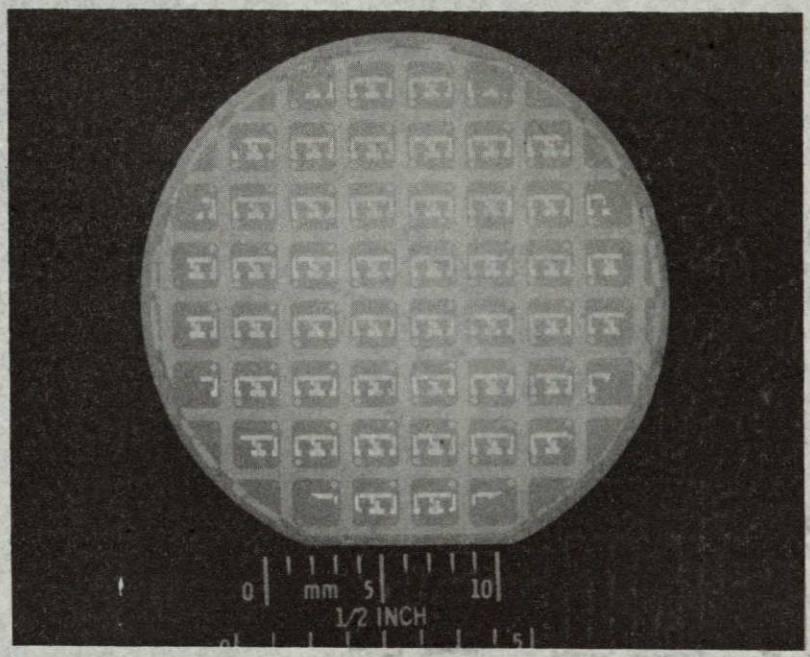


Figure 13.- Typical production wafer.

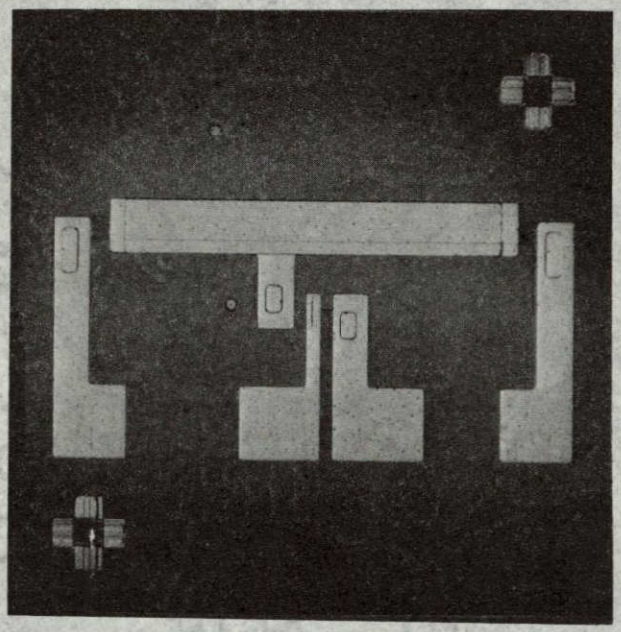


Figure 14.- Typical production die.

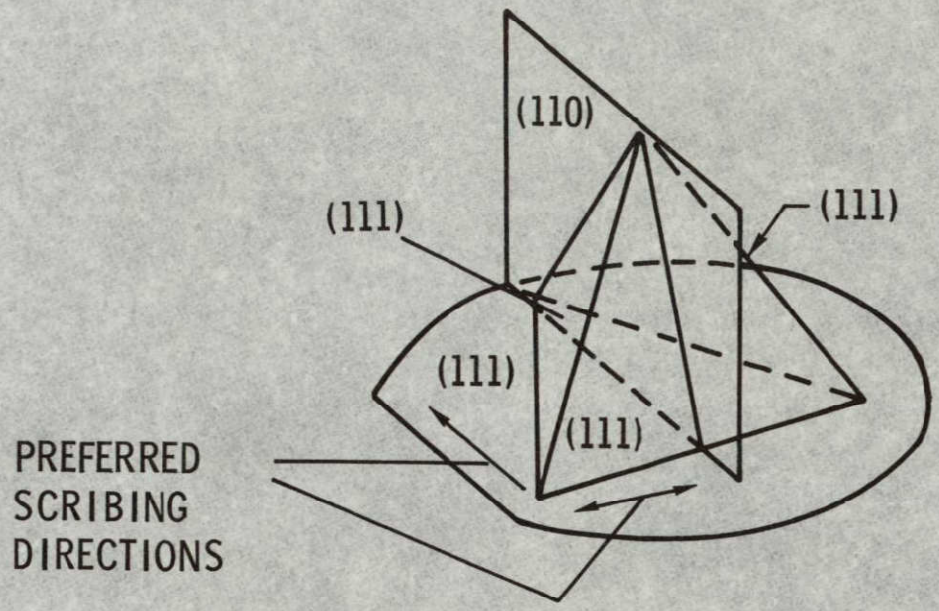


Figure 15.- Scribing Orientation[19].

and the wires were 2 mil gold. The apparatus used was manufactured by Hughes Semiconductor Inc., and the bonding pressure was approximately 400 grams with a heating cycle duration of 1000 milliseconds. The headers were only covered, but were not sealed for testing purposes. A picture of the header and bonded dice is included as Figure 16. Ten devices from the first run were carried to the phase of testing.

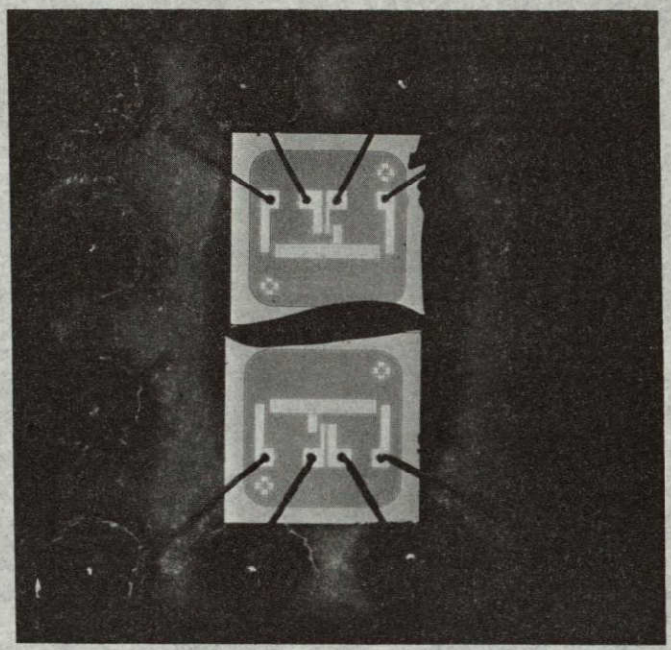


Figure 16.- Header with dice and bonds.

CHAPTER IV

TESTING, RESULTS AND CONCLUSIONS

Testing of the First Lot of Devices

The first production of devices were tested in a configuration schematically represented in Figure 17. The initial results were discouraging. The bias voltage V_A could be made no more positive than 2.5 V without unusually large current of flowing from the bias supply. This indicated a problem, since a minimal planned voltage was over the range of 0-50 volts which is normally used for cases of diode isolation to substrate. Since the only bias current expected to flow was through diode leakage only, a few microamperes was the maximum expected flow. It was obvious from the insensitivity of this bias voltage maximum to changes in the voltage of bias supply V_B that the shunt MOS device was not being turned on, and then its source diffusion was really isolated from the substrate by a very leaky diode. This prompted investigation of the diode characteristics to substrate of three externally accessible source-drain diffusion areas. On a current-voltage curve tracer all the diode isolation diffusions to substrate were identical, in spite of their different geometry, all breaking down strongly at a reverse bias of 2.5 volts, and giving indications of avalanching at approximately 6 volts, with forward conduction looking resistive. Photographs of these diode curves are included as Figure 18. The only two port measurement remaining was to measure the MOS capacitance as a function of applied bias voltage between the accessible gate

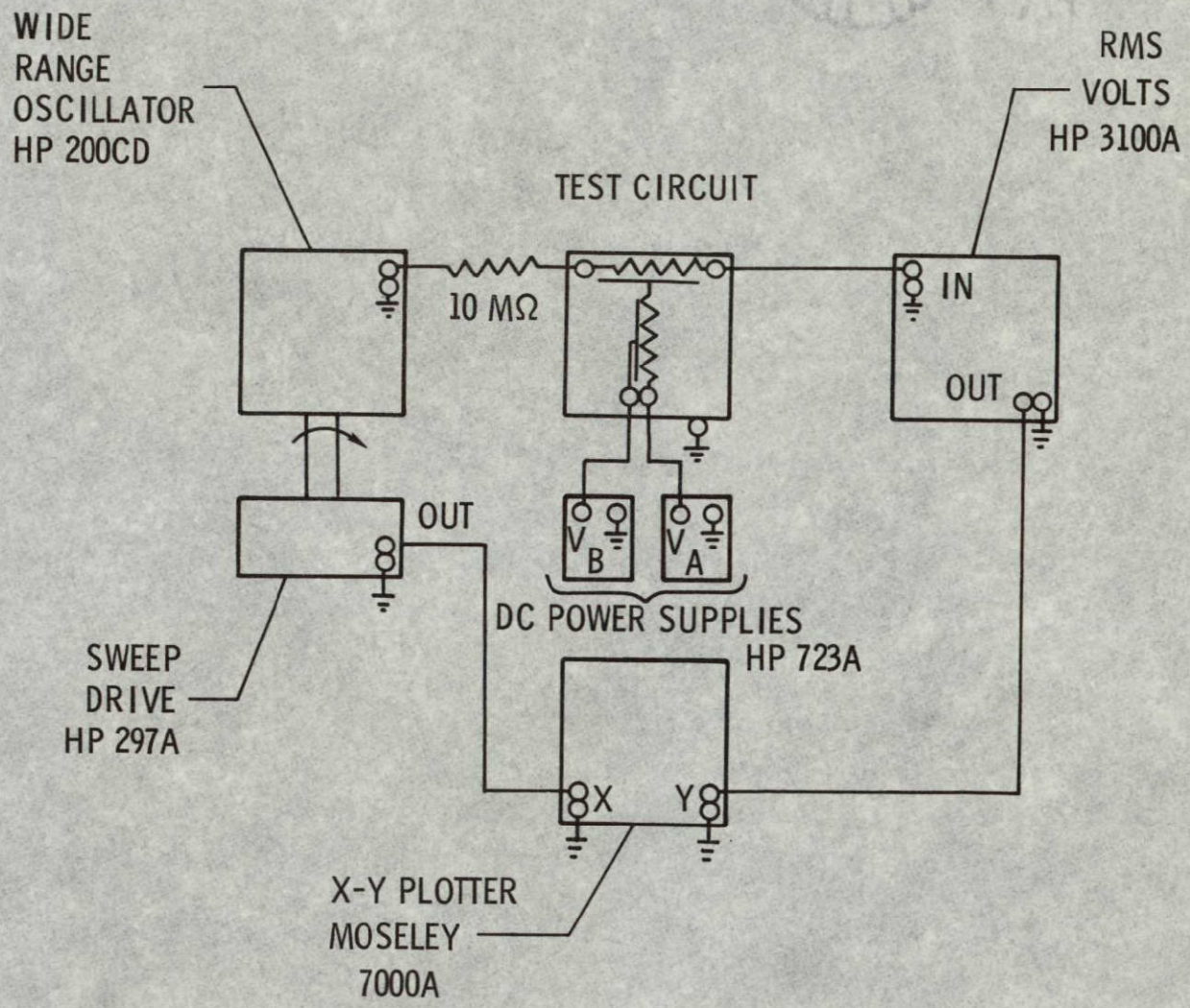
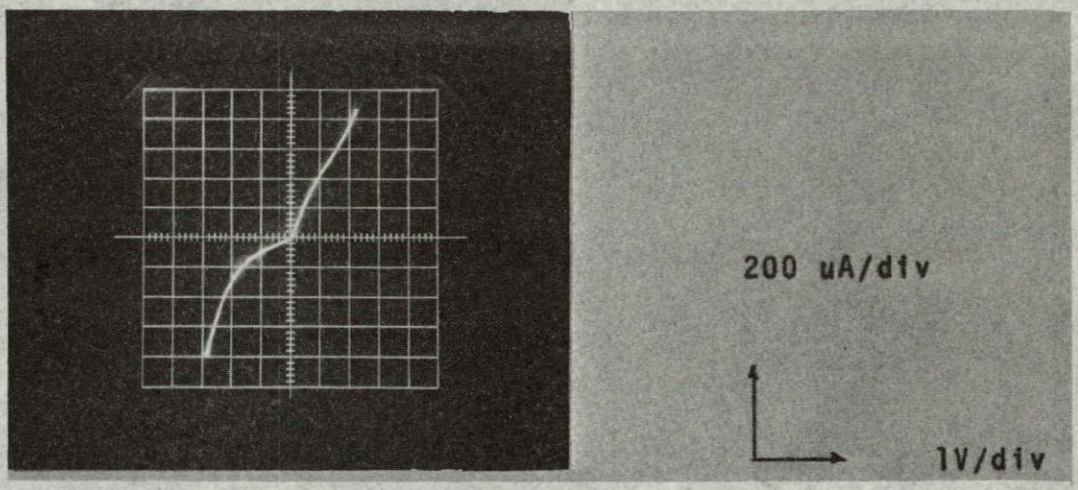
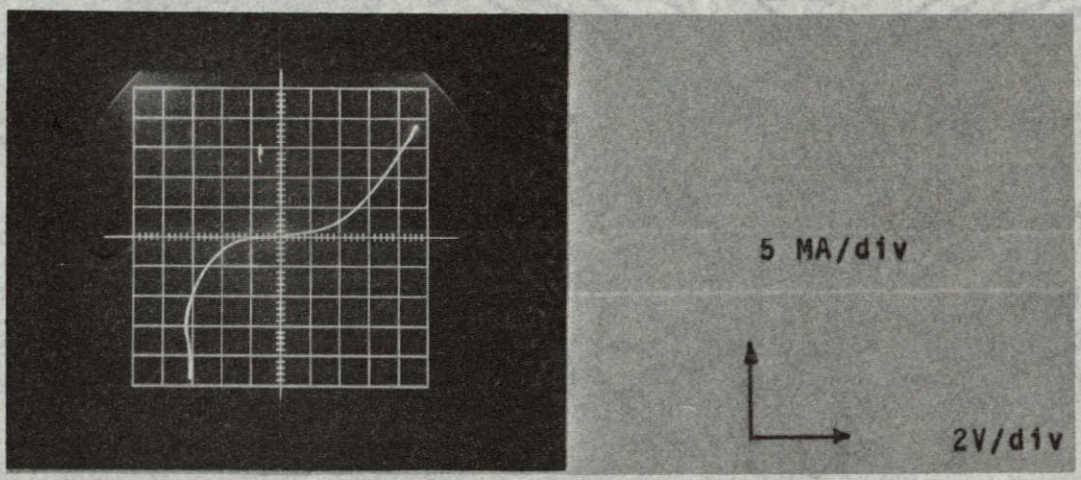


Figure 17.- Connection diagram of test apparatus.



(a) Small signal diode curve.



(b) Large signal diode curve.

Figure 18.- Diode characteristic curves.

of the shunting MOS device and the substrate. The MOS capacitance versus voltage curve was taken with the instrumentation pictured in the schematic as Figure 19. The first curve that was taken is presented as curve (a) in Figure 20. The frequency used was 1 Mhz and the curve was wholly different than was expected. Capacitance was expected to decrease to a constant value with increasing positive bias since the material underlying the metallization was expected to be the p-type host substrate except in the insignificantly small areas where the metallization overlay the small source-drain diffusion. It was further expected to be a larger constant for all negative bias. As may be noted from Figure 20(a), the opposite seemed to be the fact. In addition the minimum value of the capacitance was approximately three times the expected value. In general, this curve required that the material directly beneath the insulating oxide and also beneath all the metallization be n-type, but since the host substrate was known to be p-type, then the diffusion step in fabrication must have been excessive and impurities must have diffused through the oxide diffusion mask to such an extent so as to have made a large area planar diode beneath the surface of the oxide insulator. At this point the analysis must be widened in scope to note the appearance of the "hump" in the capacitance versus voltage curve for negative bias. Indeed, if a negative current was allowed to flow into the two terminal device, the bias voltage would become more negative, but simultaneously the capacitance would rise. These occurrences seemed to indicate two effects. The first that there was an interface charging and possibly retaining charge, and secondly that

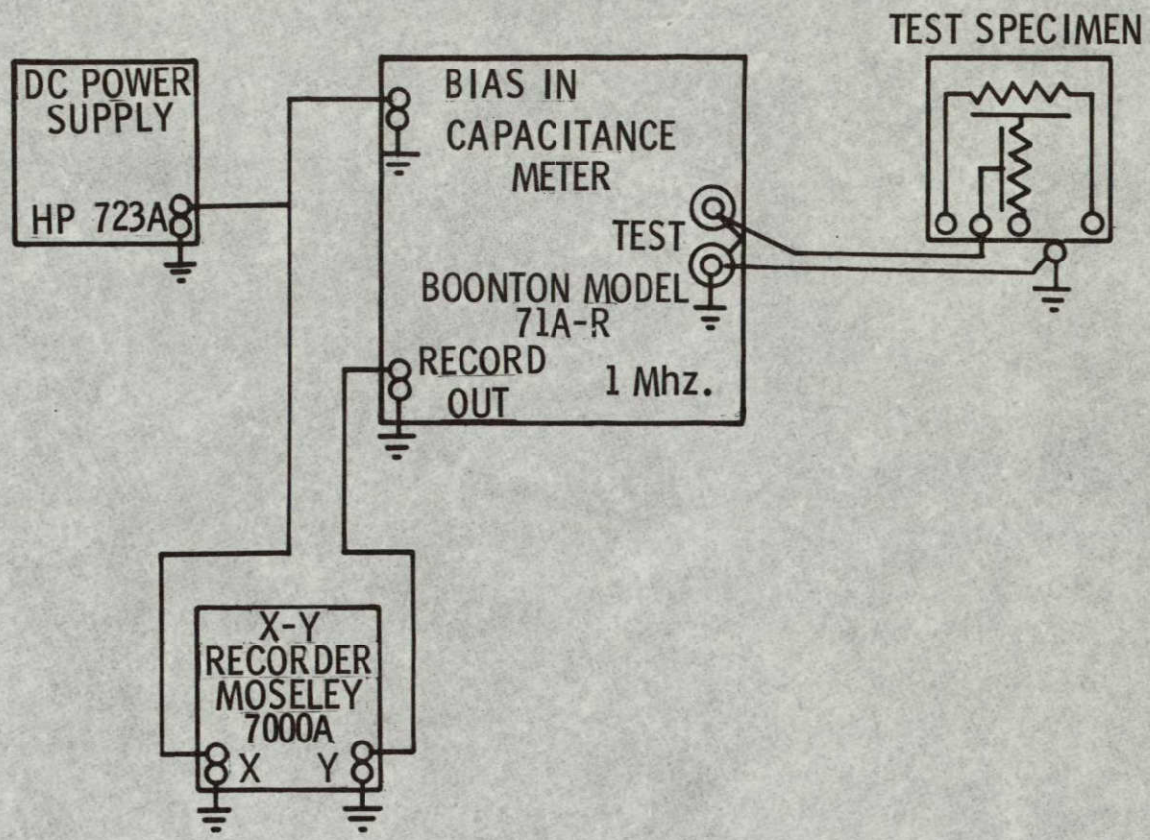


Figure 19.- Connection diagram of MOS capacitance versus voltage measurements.

there was possibly a breakdown accompanying this charging. With successive applied stresses by bias increases, the capacitance versus voltage curve shifted to the one pictured in Figure 20(b).

The next two approaches that seemed to offer insight into these problems were to first look at the network topology, and secondly to examine the electrically different areas underlying the protecting oxide, and search for a fabrication error. The picture presented as Figure 21 is the topological data measured with a Leitz multiple beam interference microscope. If this photograph is compared with the one in Figure 14, the area shown is almost in the center of the device, and represents all of the topological data on the entire wafer. The area shown is the aluminum of the series element gate where it first overlays the gate (arrow A), then the channel isolation region (arrow B), then the diffusion masking oxide (arrow C), then the diffusion oxide regrowth (arrow D), and finally where it contacts the silicon substrate (arrow E). The topological data in Figure 21(b) indicates that the masking oxide was roughly one-third the thickness expected. The diffusion masking had therefore most likely not provided a sufficient barrier to the diffusing phosphorous atoms. At this point, it seemed necessary to bevel the one remaining unbroken wafer and to define the junctions by staining. The wafer was beveled by grinding it with wet Linde metallurgical grade alumina abrasive of 0.058 micron particle size. The apparatus used to grind the wafer was a Micro Tech beveling machine with a one inch diameter mandrel. Figure 22 is included to explain where the bevel is located on the wafer. Figure 22(a) shows

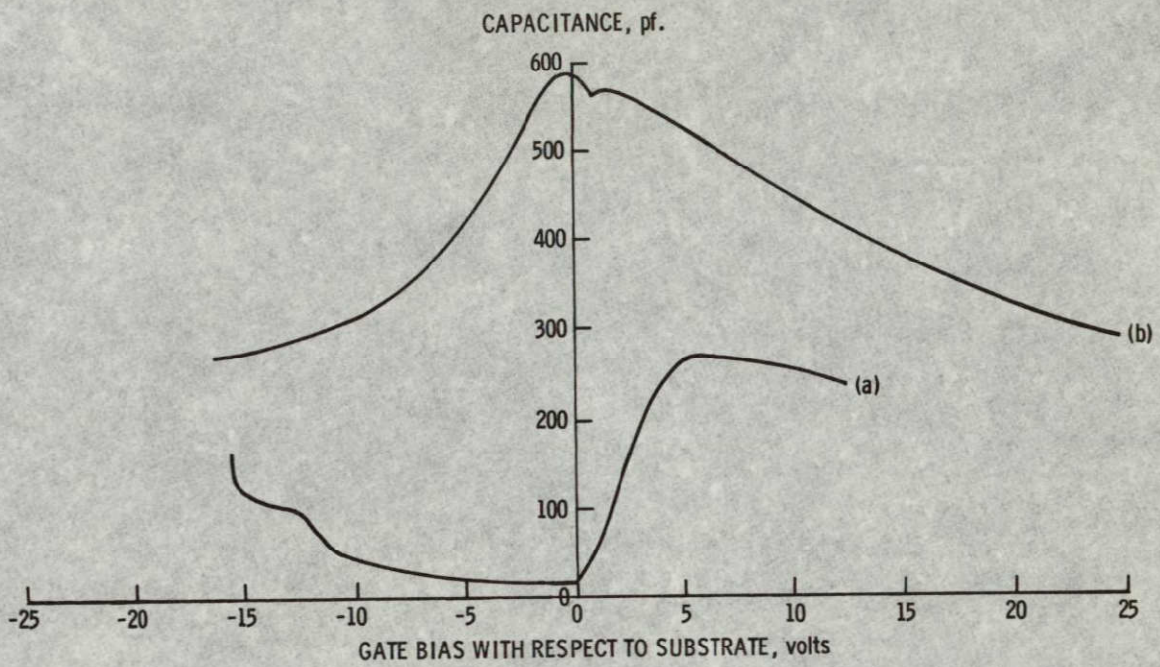
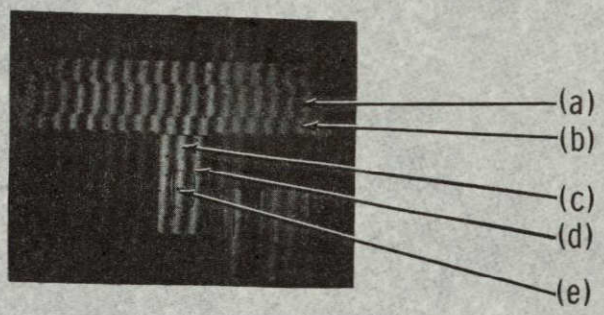
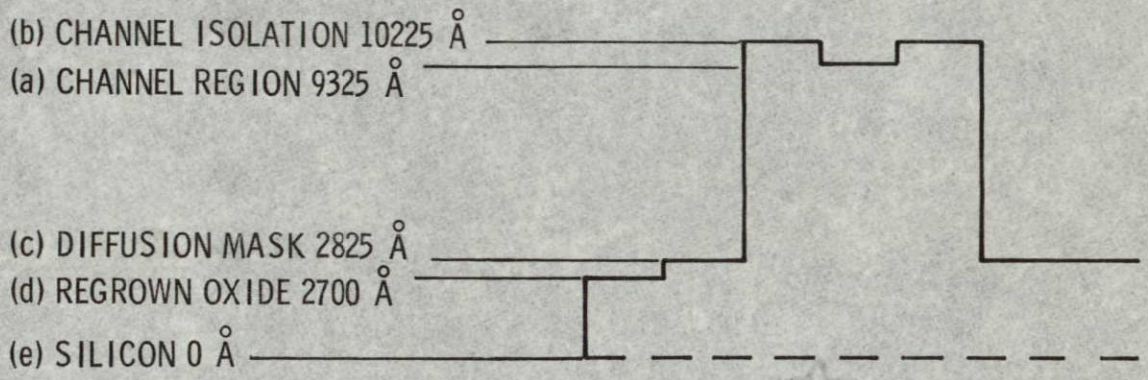


Figure 20.- Two MOS capacitance versus voltage curves.



(a) Experimental data.

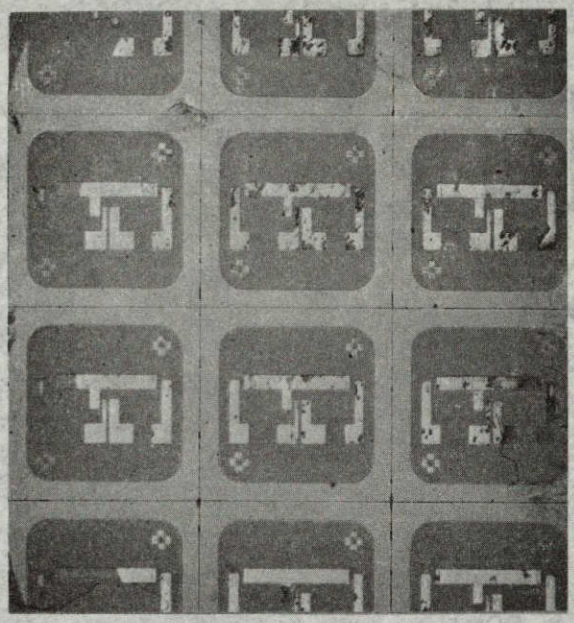


(b) Reduced data indicating topological form.

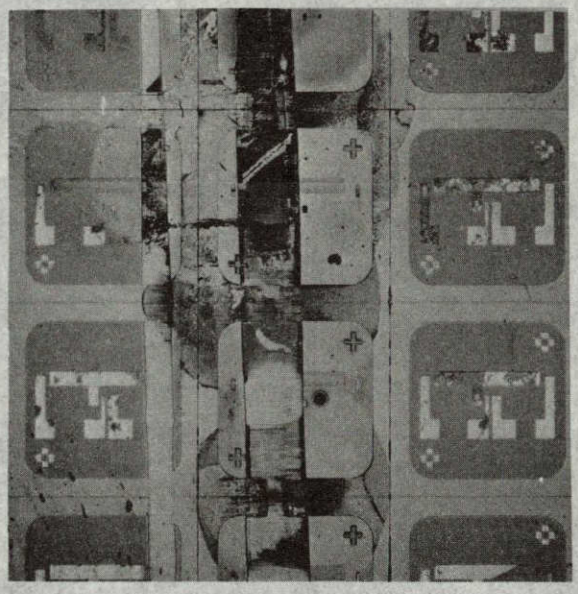
Figure 21.- Topological data.

the overall device pattern on the wafer, and 22(b) shows the area of the bevel to the same scale. Figure 23(a) shows an expanded bright field photograph of the bevel area and 23(b) shows the junctions stained by the copper acid sulfate plating solution described by Turner.[20] The n-regions are shown as bright shiny copper surfaces. From the geometry of the bevel and measurements taken it is computed that there are essentially two junctions in the structure; the first is 4.5μ deep where the n-diffusion was expected, and the second is 1.3μ deep where the mask was expected to protect the substrate against diffusion. On the lower right hand edge of the bevel in Figure 23(b), it is also noticeable that the channel oxide area is the only area where the oxide was not broken through by diffusion. For these reasons then it is clear that the first etch was therefore in error and caused failure for the lot. The first etch was grossly too deep and left the remaining oxide, which was to be the diffusion mask, too thin. The presence of a large area junction has led towards the solution of the two still unresolved problems, the unusual diode curves and the MOS capacitance versus voltage plot.

D. J. Fitzgerald and A. S. Grove[21] present a model and experimental data for junction breakdown under the influence of a gate with an applied bias. They examine a p-n junction with a transverse field induced junction. They present models for the carrier generation and junction capacitance effects and discuss their experimental results. The problem of the broken through diffusion mask is similar to their work. In this case, however, there is essentially one large area p-n

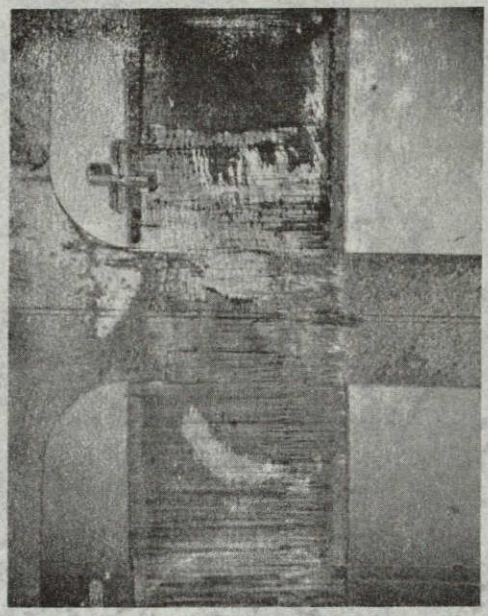


(a) General topology.

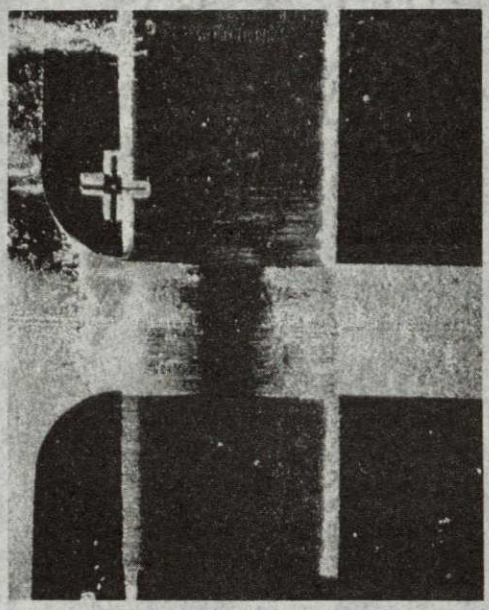


(b) Topology at bevel.

Figure 22.- Overview of topology.



(a) Bright field - not stained.

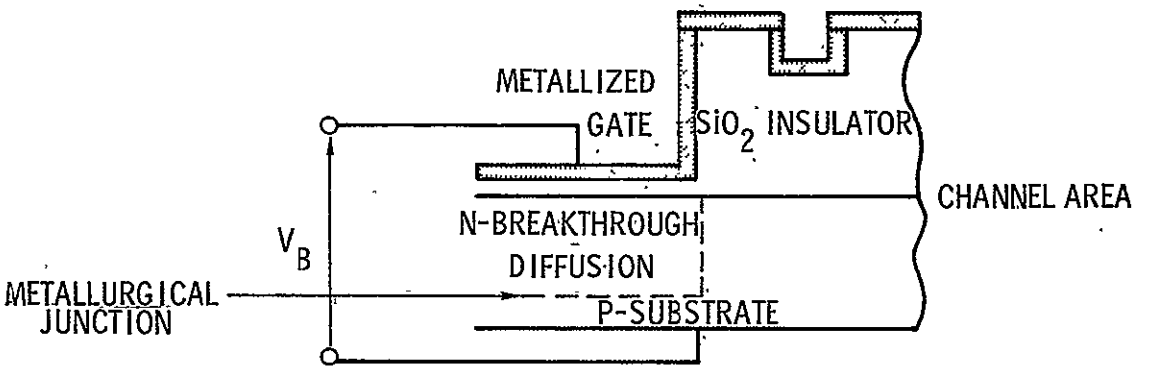


(b) Dark field - stained.

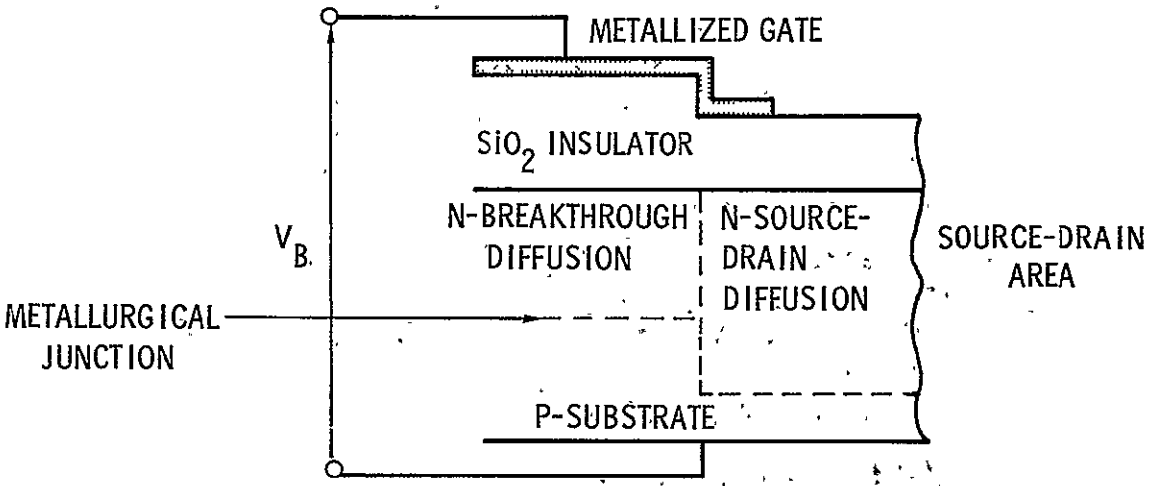
Figure 23.- Bevel and junction delineation.

junction which is parallel in space to the gate and extends to the cleaved edges of the individual die. In addition, there is a region where the gate overlays the combination of the broken through diffusion mask and the channel oxide which has not been broken through by diffusion. Both structures are outlined in cross section in Figure 24. Under negative bias stress an inversion layer is expected to appear beneath the gate as in Figure 25. From Figure 25(a) it is noticed that beneath the gate, where it overlays metallurgical junction, that any inversion layer which develops in the n-region is immediately shorted directly to the substrate through the metallurgical junction whose surface is then inverted. In this configuration, which is really the exception stated by Fitzgerald and Grove, large "channel" currents flow into the inversion regime to satisfy the charge balance, and thereby charge up the interface. On the removal of the negative gate bias potential, this positive charge possibly remains trapped at the interface and contributes towards a significantly larger capacitance. It is typical for this "channel" current to flow at a gate bias voltage of the order of tens of volts for the thickness of oxides used, and in fact it does as evidenced by the translation of the capacitance versus voltage curve in Figure 20 and the absolute increasing capacitance. This explains the fivefold increase of capacitance after potential stress and the capacitance versus voltage curve instability in the range of -15 to -20 volts.

The low reverse bias breakdowns of the source-drain diodes to the substrate may be explained in part by considering the large surface

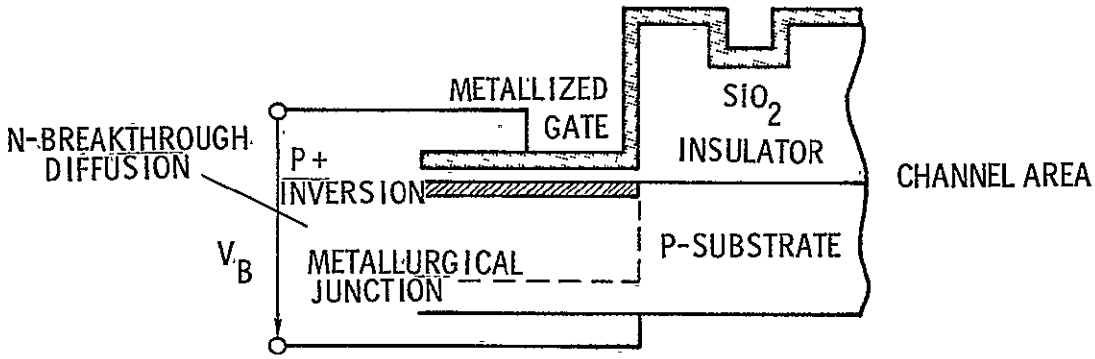


(a) Channel area cross section.

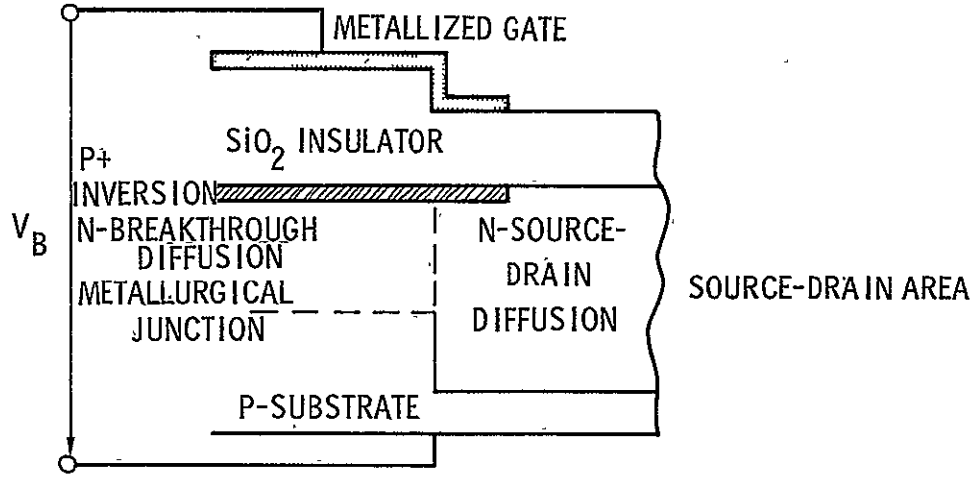


(b) Source-drain area cross section.

Figure 24.- First production diffusion breakthrough diagram.



(a) Channel area cross section.



(b) Source drain area cross section.

Figure 25.- Inversion layer development under applied bias.

area of the actual physical junctions. These source drain diffusions are connected physically to the breakthrough diffusion and then further to the cleaved edges of the die. This junction would then have a surface area of 0.01 square inches which is considerable, and in addition it would be connected directly to the scribed and broken edges which add to a total length of 0.4 inches. Fitzgerald and Grove, in the already cited Reference,[21] describe this region as a very intense region of dislocation defects and characterized by an extremely high carrier generation rate. It is proposed that these edges, where the extreme damage is, and where the junction has been scribed and broken through are the sites that cause the poor diode characteristics.

From this failure, it is recommended that more care be taken in calibration of etches, and simultaneously by checking one substrate from each processing batch to be certain that the step was correct prior to subsequent processing, which may be then altered to accomodate etching problems.

Testing of the Second Lot of Devices

A second batch of 24 wafers was processed following the same procedures as outlined for the first lot except that the first etch for one sample was checked to be sure that 2000 Å of oxide was removed prior to further processing. The diffusion for another sample was also checked by beveling and staining prior to subsequent processing. Ten wafers remained at the conclusion of processing. The insulating oxides were checked to be insulating, and the source drain diffusions were

checked to have reverse leakages in the order of microamperes to approximately 30 volts reverse bias. Testing was initiated on one of the successful chips and a voltage dependent null was found. The data was collected with apparatus conceptually similar to that in Figure 17. The exceptions were that V_A and V_B were both set with Fluke Voltage/Current Calibrators, Model No. 382A, and the oscillator used was a Hewlett-Packard Signal Generator, Model 606A. The data was taken by first setting the frequency, then nulling the detector by adjusting the bias supplies. The actual test data has been tabulated in Appendix G and the frequency versus bias voltage relationship has been plotted as Figure 26. A least squares analysis was done on the data to find the dependence of the bias voltages on the null frequencies for the one device tested. These linear dependencies and the correlation coefficients are also found on Figure 26.

This data indicates two unexpected results. The effective circuit Q is much lower than was expected, and the two bias curves are neither coincident nor parallel. The lack of coincidence and parallelism may be explained on a geometrical basis. Dimensional stability was apparently not maintained through processing, and therefore the shapes of the curves are substantially different than expected. The low effective Q, however, cannot be readily explained, except to note that even for signal levels of the order of half a volt, that 60 db below this is in the tens of microvolt range and such detection levels are difficult because of the limited dynamic range available. That is, if more resolution above the noise level would have been available at the

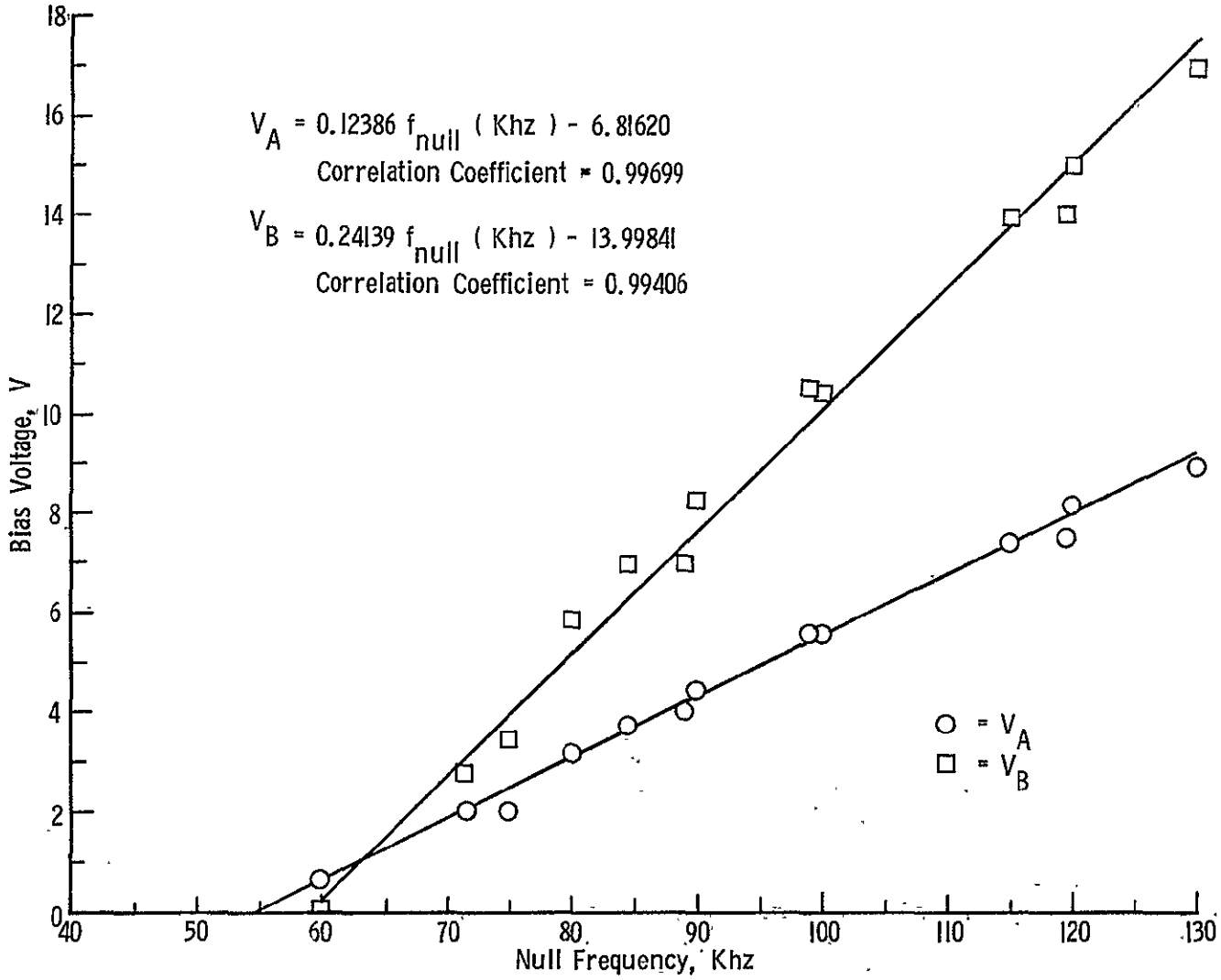


Figure 26.- Bias versus frequency

detector, the null could possibly have been adjusted sharper, then the Q would have been higher. Such work has not been done to date of this thesis.

Conclusions and Recommendations

From this work it has been demonstrated that the tunable "novel" distributed R-C notch filter may be reasonably physically approximated by a pair of suitably designed and fabricated field effect transistors which are used as variable resistance-constant capacitance distributed elements.

It is strongly recommended that this work be carried to a successful conclusion. It is recommended that, first, work be done towards further quantitative evaluation of the apparently successful prototype test specimen, then work be done towards use of this new device as a discrete five terminal network in practical circuits, and finally work be done to incorporate this new device into special purpose integrated circuitry.

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APPENDIX A

COMPUTER LISTING OF DLANET

```
      FUNCTION XL4(N,LO,LP)
      AN=N
      ALO=LO
      ALP=LP
      AA=AN/ALP+ALO
      IF (AA) 100,100,105
  100 XL4=1./10.**(-AA)
      GO TO 110
  105 XL4=10.**AA
  110 N=N+1
      RETURN
      END
      SUBROUTINE PLOT (Y,M,NF,NS)
C     SUBROUTINE FOR PLOTTING 5 X 100 INPUT ARRAY (FORTRAN 4)
      DIMENSION Y(5,100), LINE(101),L(11),JL(5)
      DATA (JL(I),I=1,5)/1HA,1HB,1HC,1HD,1HE/,JN,JP,JI,JBLANK,JZ/
     11H-,1H+,1HI,1H ,1H$/
      DO 99 I=1,101
      LINE(I)=JBLANK
   99 CONTINUE
      N=0
C     PRINT ORDINATE SCALE
      DO 101 I=1,11
      L(I)=10*I-110+NS
  101 CONTINUE
      WRITE (7,105) (L(I),I=1,11)
  105 FORMAT (3X,11(I4,6X),6HY(1,I))
      GO TO 115
  110 IF (N/10-(N-1)/10) 125,125,115
C     CONSTRUCT ORDINATE GRAPH LINE
  115 ND=0
      DO 120 I=1,10
      ND=ND+1
      LINE(ND)=JP
      DO 120 J=1,9
      ND=ND+1
  120 LINE(ND)=JN
      LINE(101)=JP
      IF (N) 135,121,135
  121 WRITE (7,170) N,LINE
      GO TO 185
C     CONSTRUCT 1 LINE OF ABSCISSA GRAPH LINES
  125 DO 130 I=1,101,10
      LINE(I)=JI
  130 CONTINUE
C     CHANGE NUMERICAL DATA TO LETTERS
  135 DO 160 I=1,M
      XNS=NS
      JA=Y(I,N)+101.49999-XNS
      IF (JA-101) 140,155,145
  140 IF (JA) 150,150,155
  145 LINE(101)=JZ
      GO TO 160
  150 LINE(1)=JZ
      GO TO 160
  155 LINE(JA)=JL(I)
  160 CONTINUE
C     PRINT LINE OF DATA
      IF (N/10-(N-1)/10) 175,175,165
  165 WRITE (7,170) N,LINE,Y(1,N)
  170 FORMAT (1X,I4,101A1,1X,  E12.5)
      GO TO 185
  175 WRITE (7,180) LINE,Y(1,N)
  180 FORMAT (5X,101A1,1X,E12.5)
C     SET LINE VARIABLES TO ZERO
  185 DO 190 I=1,101
      LINE(I)=JBLANK
  190 CONTINUE
  195 N=N+1
      IF (N-NF) 110,110,200
  200 RETURN
      END
```

```
      SUBROUTINE CMRED
      COMMON YR(15,15),R(15,15),C(15,15),RD(5,50),CD(5,50),
     1NSECT(5),N1(5),N2(5),N3(5),NN,ND,RAD,KD,NREP
     2,NGAIN,NG1(5),NG2(5),NG3(5),NG4(5),JL(5),GA(5)
      COMPLEX YR
      NA=NN-NGAIN
      NZ=NN-(2+NGAIN)
      IF (NZ.LT.1) RETURN
      DO 110 K=1,NZ
      NP=NA-1
      DO 105 J=1,NP
      DO 105 I=1,NP
      YR(I,J)=YR(I,J)-YR(I,NA)*YR(NA,J)/YR(NA,NA)
  105 CONTINUE
  110 NA=NA-1
      RETURN
      END
      SUBROUTINE YDIST
      COMMON YR(15,15),R(15,15),C(15,15),RD(5,50),CD(5,50),
     1NSECT(5),N1(5),N2(5),N3(5),NN,ND,RAD,KD,NREP
     2,NGAIN,NG1(5),NG2(5),NG3(5),NG4(5),JL(5),GA(5)
      COMPLEX YR
      COMPLEX AR(2,2),BR(2,2),CR(2,2),DR,ER,GR
      KK=NSECT(KD)
      IF (KK) 121,121,109
  109 DO 112 I=1,2
      DO 110 J=1,2
  110 CR(I,J)=(0.,0.)
  112 CR(I,I)=(1.,0.)
      DO 120 I=1,KK
      DO 115 IA=1,2
      DO 115 IB=1,2
      AR(IA,IB)=CR(IA,IB)
  115 CONTINUE
      BR(1,1)=CMPLX(1.,CD(KD,I)*RD(KD,I)*RAD)
      BR(1,2)=CMPLX (RD(KD,I),0.)
      BR(2,1)=CMPLX (0.,CD(KD,I)*RAD)
      BR(2,2)=(1.,0.)
      CR(1,1)=AR(1,1)*BR(1,1)+AR(1,2)*BR(2,1)
      CR(1,2)=AR(1,1)*BR(1,2)+AR(1,2)*BR(2,2)
      CR(2,1)=AR(2,1)*BR(1,1)+AR(2,2)*BR(2,1)
      CR(2,2)=AR(2,1)*BR(1,2)+AR(2,2)*BR(2,2)
  120 CONTINUE
      DR=(1.,0.)/CR(1,2)
      ER=DR*CR(2,2)
      GR=DR*CR(1,1)
  121 L=N1(KD)
      M=N2(KD)
      N=N3(KD)
      YR(L,L)=ER+YR(L,L)
      YR(M,M)=GR+YR(M,M)
      YR(L,M)=-DR+YR(L,M)
      YR(M,L)=YR(L,M)
      YR(N,L)=DR-ER+YR(N,L)
      YR(L,N)=YR(N,L)
      YR(N,M)=DR-GR+YR(N,M)
      YR(M,N)=YR(N,M)
      YR(N,N)=ER+GR-(2.,0.)*DR+YR(N,N)
      RETURN
      END
```

```
      SUBROUTINE CONST
C     LPH SUBROUTINE 235 REPLACES PERRY 233, JULY 1998
      COMMON YR(15,15),R(15,15),C(15,15),RD(5,50),CD(5,50),
     1NSECT(5),N1(5),N2(5),N3(5),NN,ND,RAD,KD,NREP
     2,NGAIN,NG1(5),NG2(5),NG3(5),NG4(5),JL(5),GA(5)
      COMPLEX YR
      DIMENSION NRE(15),NCE(15)
      IF (NREP.GT.0) GO TO 121
      NM=NN-NGAIN
      DO 110 I=1,NN
      NRE(I)=0
  110 NCE(I)=0
      DO 120 J=1,NGAIN
      DO 120 I=1,NN
      IF (I.EQ.NG1(J)) NRE(I)=1
      IF (I.EQ.JL(J)) NCE(I)=1
  120 CONTINUE
  121 IN=1
      DO 145 I=1,NM
  123 IF (NRE(IN)) 130,130,125
  125 IN=IN+1
      GO TO 123
  130 IF (IN.EQ.I) GO TO 140
  132 DO 135 J=1,NN
  135 YR(I,J)=YR(IN,J)
  140 IN=IN+1
  145 CONTINUE
      DO 165 I=1,NGAIN
      K=NG1(I)
      L=NG3(I)
      M=JL(I)
      IF (L.EQ.M) GO TO 155
      DO 150 J=1,NM
  150 YR(J,L)=YR(J,L)+YR(J,K)*GA(I)
      GO TO 165
  155 DO 160 J=1,NM
  160 YR(J,K)=YR(J,K)+YR(J,L)/GA(I)
  165 CONTINUE
      IN=1
      DO 190 I=1,NM
  172 IF (NCE(IN)) 175,175,170
  170 IN=IN+1
      GO TO 172
  175 IF (IN.EQ.I) GO TO 185
      DO 180 J=1,NM
  180 YR(J,I)=YR(J,IN)
  185 IN=IN+1
  190 CONTINUE
      RETURN
      END
```

```
      SUBROUTINE DISRP
      COMMON YR(15,15),R(15,15),C(15,15),RD(5,50),CD(5,50),
     1NSECT(5),N1(5),N2(5),N3(5),NN,ND,RAD,KD,NREP
     2,NGAIN,NG1(5),NG2(5),NG3(5),NG4(5),JL(5),GA(5)
      COMPLEX YR
      DIMENSION P(10)
      DO 199 I=1,ND
      READ 150,NOPT,NSECT(I),N1(I),N2(I),N3(I)
  150 FORMAT (5I3)
      PRINT 155,I,NSECT(I),N1(I),N2(I),N3(I)
  155 FORMAT (1HO,19HDISTRIBUTED NETWORK,I2,5X,I3,9H SECTIONS,5X,
     1  18HCONNECTED TO NODES,3I3)
      NZ=NSECT(I)
      IF (NZ) 156,156,159
  156 PRINT 157
  157 FORMAT (1HO,20X,21HSEE PRECEDING NETWORK)
      GO TO 199
  159 DIV=NZ
      GO TO (160,180,190,200),NOPT
  160 READ 165,RT,CT
  165 FORMAT (8E10.0)
      PRINT 170,RT,CT
  170 FORMAT(1HO,17HTOTAL RESISTANCE=,  E15.8,5X,18HTOTAL CAPACITANCE=,
     1  E15.8)
      RT=RT/DIV
      CT=CT/DIV
      DO 175 IA=1,NZ
      RD(I,IA)=RT
  175 CD(I,IA)=CT
      PRINT 176,RT,CT
  176 FORMAT(1HO,17HRESISTANCE/SECT.=,  E15.8,5X,
     1  18HCAPACITANCE/SECT.=,E15.8)
      GO TO 199
  180 READ 165,ALF,RA,RB,CA,CB
      IF (ALF) 182,182,185
  182 IF (RB) 184,184,183
  183 ALF=ALOG  (RB)-ALOG  (RA)
      GO TO 185
  184 ALF=ALOG  (CA)-ALOG  (CB)
  185 DIV=DIV-1.
      DO 188 IA=1,NZ
      DIA=IA-1
      DB=ALF*DIA/DIV
      RD(I,IA)=RA*EXP  (DB)
  188 CD(I,IA)=CA*EXP  (-DB)
      PRINT 189,ALF
  189 FORMAT (1HO,17HEXPONENTIAL TAPER,1X,7HALPHA =,E17.8)
      GO TO 191
  190 READ 165,  (RD(I,IA),IA=1,NZ)
      READ 165,  (CD(I,IA),IA=1,NZ)
      GO TO 191
  200 PRINT 202.
  202 FORMAT (1HO,42HPOLYNOMIAL TAPER, R(X)=R*POLY, C(X)=C/POLY   )
      READ 201,NP,RI,CI,XT
  201 FORMAT (I3,7X,7F10.0)
      READ 165,(P(I),I=1,NP)
      PRINT 205,NP
  205 FORMAT(1HO,I2,47H COEFFICIENTS P(I) OF POLY 1+P(1)X+P(2)X**2+.../)
      PRINT 193, (P(I),I=1,NP)
      PRINT 210,XT,RI,CI
  210 FORMAT (1HO,10HLENGTH  X=,  E10.3,5X,10HINITIAL R=,E10.3,
     15X,*INITIAL C=*E10.3)
      DO 220 IA=1,NZ
      PIA=IA
      X=PIA*XT/DIV
      AP=1.
      DO 215 IB=1,NP
      AP=AP+P(IB)*X**IB
  215 CONTINUE
      RD(I,IA)=RI*AP
  220 CD(I,IA)=CI/AP
  191 PRINT 192
  192 FORMAT (1HO,18hRESISTANCE/SECTION)
      PRINT 193, (RD(I,IA),IA=1,NZ)
```

```
  193 FORMAT (1X,  7E17.8)
      PRINT 194
  194 FORMAT (1HO,19HCAPACITANCE/SECTION)
      PRINT 193, (CD(I,IA),IA=1,NZ)
  199 CONTINUE
      RETURN
      END
      PROGRAM MAIN (INPUT,OUTPUT,PUNCH,TAPE4=INPUT,TAPE7)
C     MAIN PROGRAM, CLA NETWORK ANALYSIS,5VCVS VERSION
      COMMON YR(15,15),R(15,15),C(15,15),RD(5,50),CD(5,50),
     1NSECT(5),N1(5),N2(5),N3(5),NN,ND,RAD,KD,NREP
     2,NGAIN,NG1(5),NG2(5),NG3(5),NG4(5),JL(5),GA(5)
      COMPLEX YR
      DIMENSION Y(5,100),LTR(8),Z(5,100)
      COMPLEX VD
      READ 99,LTR
   99 FORMAT (8A10)
      JX=1
   96 PRINT 98,LTR
   98 FORMAT (1H1,8A10)
  102 NREP=0
      PHSD=0.
      IX=0
      READ 107,NN,ND,NF,NSY,NSP,KRAD,LMAG,LPHS,KPLT,LFRQ,OLDG,FA,FB,
     1SCALE,SCALP,KPUN,NGAIN
  107 FORMAT (5I3,5I1,5E10.0,I1,I3)
      PRINT 106,JX
  106 FORMAT (/1HO,14HPROBLEM NUMBER,I2)
      PRINT 110,NN,ND
  110 FORMAT(1HO,I2,6H NODES,5X,I2,24H DISTRIBUTED SUBNETWORKS)
      DO 101 I=1,NN
      DO 101 J=1,NN
      R(I,J)=0.
  101 C(I,J)=0.
      IF (NGAIN.GT.0) GO TO 95
      NGAIN=1
      NG1(1)=2
      NG2(1)=0
      NG3(1)=3
      NG4(1)=0
      JL(1)=3
      GA(1)=OLDG
      GO TO 92
   95 DO 94 I=1,NGAIN
   94 READ 93,NG1(I),NG2(I),NG3(I),NG4(I),JL(I),GA(I)
   93 FORMAT (5I3,5X,F10.0)
   92 PRINT 91,NGAIN
   91 FORMAT (1HO,I2,1X,*GAIN ELEMENTS OF VCVS TYPE*)
      PRINT 90,(I,NG1(I),NG2(I),NG3(I),NG4(I),JL(I),GA(I),I=1,NGAIN)
   90 FORMAT (1X*NO.*I2*, SOURCE AT NODES*I3,2H -,I3
     1*, CONTROL VOLTAGE AT NODES*I3,2H -,I3*, SUPRESS NODE*I3
     2*, GAIN=*E12.5)
      PRINT 115
  115 FORMAT (1HO,15HLUMPED ELEMENTS)
   13 PRINT 116
  116 FORMAT (5X,5HNODES,8X,7HR(OHMS),8X,9HC(FARADS))
  113 READ 105,I,J,RA,CA
  105 FORMAT (2I2,6X,2E10.0)
      IF (I) 112,112,111
  111 PRINT 114,I,J,RA,CA
  114 FORMAT (1X,2I5,  2E15.3)
      IF (RA) 104,103,104
  104 RA=1./RA
      IF (J.EQ.0) GO TO 14
      R(J,J)=RA+R(J,J)
      R(I,J)=-RA+R(I,J)
      R(J,I)=R(I,J)
   14 R(I,I)=RA+R(I,I)
  103 IF (CA.EQ.0.) GO TO 113
      IF (J.EQ.0) GO TO 15
      C(J,J)=CA+C(J,J)
      C(I,J)=-CA+C(I,J)
      C(J,I)=C(I,J)
   15 C(I,I)=CA+C(I,I)
      GO TO 113
  112 IF (NREP.GT.0) GO TO 124
  118 CALL DISRP
```

```
    IF (NREP.GT.0) GO TO 124
117 IF(KRAD) 160,160,161
160 PRINT 162
162 FORMAT (1HO,40HVALUES OF FREQUENCY ARE IN HERTZ
    GO TO 165
161 PRINT 163
163 FORMAT (1HO,41HVALUES OF FREQUENCY ARE IN RADIANS/SECOND
165 IF (LFRQ) 120,120,122
120 PRINT 121,NF,FA,FB
121 FORMAT( 1HO,16HLINEAR FREQ PLOT,I4,12H POINTS FROM,  E15.8,4H TO
   1  E15.8)
    DNF=NF
    FREQ=FA
    DF=(FB-FA)/DNF
    GO TO 124
122 IF(FA-1.) 150,151,151
151 FL=ALOG10 (FA)
    GO TO 152
150 FL=-ALOG10 (1./(FA-.0001))
152 LOG1=FL
    IF (FB-1.) 153,154,154
154 FM=ALOG10 (FB)
    GO TO 155
153 FM=-ALOG10 (1./(FB-.0001))
155 LOG2=FM
    NG=NF/(LOG2-LOG1)
    PRINT 123,NG,LOG1,LOG2
123 FORMAT( 1HO,13HLOG FREQ PLOT,I5,21H POINTS/DEC FROM 10**,I2,
   1  9H  TO 10**,I2)
    NLG=1
124 PRINT 144
144 FORMAT (1HO,3X,2HJX,3X,2HIX,8X,8HFREQ(HZ),15X,3HRAD,17X,3HVXM,15X,
   17HVXM(DB),11X,10HPHASE(DEG))
125 IF (LFRQ) 126,126,127
126 FREQ=FREQ+DF
    GO TO 128
127 FREQ=XL4(NLG,LOG1,NG)
128 IF(FREQ-FB-.0001) 129,129,139
129 IF (KRAD) 170,170,171
170 RAD=FREQ*6.283185307
    FREQH=FREQ
    GO TO 130
171 RAD=FREQ
    FREQH=FREQ/6.283185307
130 NNN=NN+1
    DO 131 I=1,NNN
    DO 131 J=1,NNN
131 YR(I,J)=(0.,0.)
    DO 132 I=1,ND
    KD=I
132 CALL YDIST
    DO 134 I=1,NN
    DO 134 J=1,NN
134 YR(I,J)=YR(I,J)+CMPLX(R(I,J),C(I,J)*RAD)
    CALL CONST
    CALL CMRED
    VD=-YR(2,1)/YR(2,2)
    VXM=CABS (VD)
    VXMDB=20.*ALOG10 (VXM)
    IX=IX+1
    IF (LPHS) 180,180,181
181 PHSD=ATAN2(AIMAG(VD),REAL(VD))*57.2957795
    Z(JX,IX)=PHSD*SCALP
180 PRINT 145,JX,IX,FREQH,RAD,VXM,VXMDB,PHSD
145 FORMAT (1X,2I5,5E20.8)
    IF (KPUN.GT.0) PUNCH 200,IX,FREQH,RAD,VXM,VXMDB,PHSD
200 FORMAT (I4,1X,5E15.8)
    IF (LMAG) 137,137,136
136 Y(JX,IX)=VXM*SCALE
    GO TO 135
137 Y(JX,IX)=VXMDB*SCALE
135 IF (IX-NF) 125,139,139
139 IX=0
    JX=JX+1
    READ 107,NREP
    IF (EOF,4) 999,193
```

```
193 IF (NREP.EQ.0) GO TO 102
    NLG=1
    FREQ=FA
    PRINT 106,JX
    GO TO (190,118,194,102  ),NREP
190 READ 191,(GA(I),I=1,NGAIN)
191 FORMAT (8E10.0)
    PRINT 89
 89 FORMAT (1HO*CHANGES IN GAIN ELEMENTS*)
    PRINT 90,(I,NG1(I),NG2(I),NG3(I),NG4(I),JL(I),GA(I),I=1,NGAIN
    GO TO 124
194 PRINT 195
195 FORMAT (1HO,26HCHANGES IN LUMPED ELEMENTS/)
    GO TO 13
999 IF (KPLT.GT.0) STOP
    IF (LMAG) 172,172,174
172 WRITE (7,173) SCALE,LTR
173 FORMAT (1H1,12HDB SCALED BY, E9.2,5X,8A10/)
    GO TO 179
174 WRITE (7,175) SCALE,LTR
175 FORMAT (1H1,13HMAG SCALED BY, E9.2,5X,8A10/)
179 JX=JX-1
    CALL PLOT (Y,JX,NF,NSY)
146 IF (LPHS) 183,183,184
184 WRITE (7,185) SCALP,LTR
185 FORMAT (1H1,21HPHASE(DEG), SCALED BY,E9.2,5X,8A10/)
    CALL PLOT (Z,JX,NF,NSP)
183 STOP
    END
```

APPENDIX B

DLANET OUTPUT FROM SIMULATIONS

1. - Tabulated Output for Idealized Case

```
DISTRIBUTED FILTER IDEALIZED CASE


 4 NODES       2 DISTRIBUTED SUBNETWORKS

 1 GAIN ELEMENTS OF VCVS TYPE
NO. 1, SOURCE AT NODES  2 -  0, CONTROL VOLTAGE AT NODES  3 -  0, SUPRESS NODE  3, GAIN= 1.00000E+00

LUMPED ELEMENTS
    NODES         R(OHMS)         C(FARADS)
```

DISTRIBUTED NETWORK 1 50 SECTIONS CONNECTED TO NODES 1 3 4

TOTAL RESISTANCE= 2.16300000E+06 TOTAL CAPACITANCE= 8.23200000E-12

RESISTANCE/SECT.= 4.32600000E+04 CAPACITANCE/SECT.= 1.64640000E-13

DISTRIBUTED NETWORK 2 50 SECTIONS CONNECTED TO NODES 4 5 5

TOTAL RESISTANCE= 1.21500000E+05 TOTAL CAPACITANCE= 1.61800000E-18

RESISTANCE/SECT.= 2.43000000E+03 CAPACITANCE/SECT.= 3.23600000E-20

IX	FREQ(HZ)	RAD	VXM	VXM(DB)	PHASE(DEG)
1	1.04712855E+04	6.57930271E+04	8.68832144E-01	-1.22128240E+00	-3.16632334E+01
2	1.09647820E+04	6.88937569E+04	8.58463034E-01	-1.32556803E+00	-3.29354300E+01
3	1.14815362E+04	7.21406196E+04	8.47455117E-01	-1.43766588E+00	-3.42417460E+01
4	1.20226443E+04	7.55405023E+04	8.35795688E-01	-1.55799748E+00	-3.55812976E+01
5	1.25892541E+04	7.91006165E+04	8.23475562E-01	-1.68698570E+00	-3.69530196E+01
6	1.31825674E+04	8.28285137E+04	8.10489483E-01	-1.82505232E+00	-3.83556665E+01
7	1.38038426E+04	8.67321013E+04	7.96836497E-01	-1.97261564E+00	-3.97878167E+01
8	1.44543977E+04	9.08196593E+04	7.82520260E-01	-2.13008819E+00	-4.12478800E+01
9	1.51356125E+04	9.50998580E+04	7.67549273E-01	-2.29787471E+00	-4.27341095E+01
10	1.58489319E+04	9.95817762E+04	7.51937038E-01	-2.47637045E+00	-4.42446159E+01
11	1.65958691E+04	1.04274921E+05	7.35702108E-01	-2.66595999E+00	-4.57773860E+01
12	1.73780083E+04	1.09189246E+05	7.18868030E-01	-2.86701661E+00	-4.73303045E+01
13	1.81970086E+04	1.14335177E+05	7.01463178E-01	-3.07990243E+00	-4.89011784E+01
14	1.90546072E+04	1.19723628E+05	6.83520478E-01	-3.30496940E+00	-5.04877632E+01
15	1.99526231E+04	1.25366029E+05	6.65077013E-01	-3.54256125E+00	-5.20877917E+01
16	2.08929613E+04	1.31274348E+05	6.46173546E-01	-3.79301652E+00	-5.36990033E+01
17	2.18776162E+04	1.37461117E+05	6.26853945E-01	-4.05667274E+00	-5.53191731E+01
18	2.29086765E+04	1.43939460E+05	6.07164548E-01	-4.33387188E+00	-5.69461414E+01
19	2.39883292E+04	1.50723118E+05	5.87153483E-01	-4.62496718E+00	-5.85778408E+01
20	2.51188643E+04	1.57826479E+05	5.66869950E-01	-4.93033129E+00	-6.02123221E+01
21	2.63026799E+04	1.65264612E+05	5.46363521E-01	-5.25036609E+00	-6.18477773E+01
22	2.75422870E+04	1.73053293E+05	5.25683440E-01	-5.58551408E+00	-6.34825588E+01
23	2.88403150E+04	1.81209044E+05	5.04877971E-01	-5.93627156E+00	-6.51151963E+01
24	3.01995172E+04	1.89749163E+05	4.83993805E-01	-6.30320394E+00	-6.67444089E+01
25	3.16227766E+04	1.98691765E+05	4.63075527E-01	-6.68696340E+00	-6.83691132E+01
26	3.31131121E+04	2.08055820E+05	4.42165176E-01	-7.08830929E+00	-6.99884285E+01
27	3.46736850E+04	2.17861188E+05	4.21301880E-01	-7.50813207E+00	-7.16016768E+01
28	3.63078055E+04	2.28128670E+05	4.00521591E-01	-7.94748135E+00	-7.32083797E+01
29	3.80189396E+04	2.38880043E+05	3.79856905E-01	-8.40759950E+00	-7.48082524E+01
30	3.98107171E+04	2.50138112E+05	3.59336969E-01	-8.88996201E+00	-7.64011933E+01
31	4.16869383E+04	2.61926759E+05	3.38987467E-01	-9.39632717E+00	-7.79872719E+01
32	4.36515832E+04	2.74270586E+05	3.18830684E-01	-9.92879778E+00	-7.95667135E+01
33	4.57088190E+04	2.87196980E+05	2.98885632E-01	-1.04898992E+01	-8.11398814E+01
34	4.78630092E+04	3.00732156E+05	2.79168230E-01	-1.10826801E+01	-8.27072577E+01
35	5.01187234E+04	3.14905226E+05	2.59691535E-01	-1.17108441E+01	-8.42694209E+01
36	5.24807460E+04	3.29746252E+05	2.40466007E-01	-1.23789261E+01	-8.58270228E+01
37	5.49540874E+04	3.45286714E+05	2.21499803E-01	-1.30925331E+01	-8.73807615E+01
38	5.75439937E+04	3.61559576E+05	2.02799091E-01	-1.38586799E+01	-8.89313521E+01
39	6.02559586E+04	3.78599354E+05	1.84368376E-01	-1.46862714E+01	-9.04794923E+01
40	6.30957344E+04	3.96442192E+05	1.66210837E-01	-1.55868133E+01	-9.20258210E+01
41	6.60693448E+04	4.15125936E+05	1.48328650E-01	-1.65754991E+01	-9.35708639E+01
42	6.91830971E+04	4.34690219E+05	1.30723318E-01	-1.76729387E+01	-9.51149555E+01
43	7.24435960E+04	4.55176538E+05	1.13395982E-01	-1.89080467E+01	-9.66581140E+01

IX	FREQ(HZ)	RAD	VXM	VXM(DB)	PHASE(DEG)
44	7.58577575E+04	4.76628347E+05	9.63477115E-02	-2.03231719E+01	-9.81998145E+01
45	7.94328235E+04	4.99091149E+05	7.95797852E-02	-2.19839448E+01	-9.97385163E+01
46	8.31763771E+04	5.22612591E+05	6.30939313E-02	-2.40002482E+01	-1.01270516E+02
47	8.70963590E+04	5.47242563E+05	4.68925499E-02	-2.65779230E+01	-1.02786552E+02
48	9.12010839E+04	5.73033311E+05	3.09789092E-02	-3.01786776E+01	-1.04258291E+02
49	9.54992586E+04	6.00039538E+05	1.53574097E-02	-3.62736406E+01	-1.05544024E+02
50	1.00000000E+05	6.28318531E+05	1.53967398E-04	-7.62514246E+01	-2.96684808E+01
51	1.04712855E+05	6.57930271E+05	1.49898350E-02	-3.64840630E+01	7.01735066E+01
52	1.09647820E+05	6.88937569E+05	2.96993459E-02	-3.05450623E+01	6.88842357E+01
53	1.14815362E+05	7.21406196E+05	4.40892726E-02	-2.71133413E+01	6.74046962E+01
54	1.20226443E+05	7.55405023E+05	5.81497805E-02	-2.47090384E+01	6.58789701E+01
55	1.25892541E+05	7.91006165E+05	7.18703372E-02	-2.28690063E+01	6.43371004E+01
56	1.31825674E+05	8.28285137E+05	8.52397791E-02	-2.13871537E+01	6.27903510E+01
57	1.38038426E+05	8.67321013E+05	9.82465275E-02	-2.01536558E+01	6.12447836E+01
58	1.44543977E+05	9.08196593E+05	1.10878856E-01	-1.91030253E+01	5.97046401E+01
59	1.51356125E+05	9.50998580E+05	1.23125188E-01	-1.81930619E+01	5.81734569E+01
60	1.58489319E+05	9.95817762E+05	1.34974421E-01	-1.73949706E+01	5.66544975E+01
61	1.65958691E+05	1.04274921E+06	1.46416257E-01	-1.66882140E+01	5.51509348E+01
62	1.73780083E+05	1.09189246E+06	1.57441544E-01	-1.60576132E+01	5.36659273E+01
63	1.81970086E+05	1.14335177E+06	1.68042598E-01	-1.54916123E+01	5.22026454E+01
64	1.90546072E+05	1.19723628E+06	1.78213518E-01	-1.49811871E+01	5.07642712E+01
65	1.99526231E+05	1.25366029E+06	1.87950472E-01	-1.45191316E+01	4.93539846E+01
66	2.08929613E+05	1.31274348E+06	1.97251943E-01	-1.40995742E+01	4.79749400E+01
67	2.18776162E+05	1.37461117E+06	2.06118943E-01	-1.37176419E+01	4.66302384E+01
68	2.29086765E+05	1.43939460E+06	2.14555175E-01	-1.33692201E+01	4.53228962E+01
69	2.39883292E+05	1.50723118E+06	2.22567150E-01	-1.30507787E+01	4.40558115E+01
70	2.51188643E+05	1.57826479E+06	2.30164255E-01	-1.27592424E+01	4.28317293E+01
71	2.63026799E+05	1.65264612E+06	2.37358762E-01	-1.24918946E+01	4.16532059E+01
72	2.75422870E+05	1.73053293E+06	2.44165797E-01	-1.22463035E+01	4.05225724E+01
73	2.88403150E+05	1.81209044E+06	2.50603248E-01	-1.20202661E+01	3.94418578E+01
74	3.01995172E+05	1.89749163E+06	2.56691634E-01	-1.18117657E+01	3.84129526E+01
75	3.16227766E+05	1.98691765E+06	2.62453916E-01	-1.16189389E+01	3.74371724E+01
76	3.31131121E+05	2.08055820E+06	2.67915269E-01	-1.14400507E+01	3.65156219E+01
77	3.46736850E+05	2.17861188E+06	2.73102803E-01	-1.12734769E+01	3.56489622E+01
78	3.63078055E+05	2.28128670E+06	2.78045245E-01	-1.11176905E+01	3.48374198E+01
79	3.80189396E+05	2.38880043E+06	2.82772576E-01	-1.09712542E+01	3.40807608E+01
80	3.98107171E+05	2.50138112E+06	2.87315626E-01	-1.08328151E+01	3.33782712E+01
81	4.16869383E+05	2.61926759E+06	2.91705648E-01	-1.07011032E+01	3.27287451E+01
82	4.36515832E+05	2.74270586E+06	2.95973848E-01	-1.05749332E+01	3.21304833E+01
83	4.57088190E+05	2.87196980E+06	3.00150911E-01	-1.04532067E+01	3.15813034E+01
84	4.78630092E+05	3.00732156E+06	3.04266513E-01	-1.03349169E+01	3.10785632E+01
85	5.01187234E+05	3.14905226E+06	3.08348841E-01	-1.02191536E+01	3.06191985E+01
86	5.24807460E+05	3.29746252E+06	3.12424142E-01	-1.01051083E+01	3.01997747E+01
87	5.49540874E+05	3.45286714E+06	3.16516297E-01	-9.99207847E+00	2.98165524E+01
88	5.75439937E+05	3.61559576E+06	3.20646466E-01	-9.87947084E+00	2.94655647E+01
89	6.02559586E+05	3.78599354E+06	3.24832792E-01	-9.76680271E+00	2.91427034E+01
90	6.30957344E+05	3.96442192E+06	3.29090194E-01	-9.65370118E+00	2.88438108E+01
91	6.60693448E+05	4.15125936E+06	3.33430253E-01	-9.53989995E+00	2.85647740E+01
92	6.91830971E+05	4.34690219E+06	3.37861200E-01	-9.42523359E+00	2.83016152E+01
93	7.24435960E+05	4.55176538E+06	3.42387996E-01	-9.30962939E+00	2.80505759E+01
94	7.58577575E+05	4.76628347E+06	3.47012516E-01	-9.19309723E+00	2.78081904E+01
95	7.94328235E+05	4.99091149E+06	3.51733812E-01	-9.07571761E+00	2.75713447E+01
96	8.31763771E+05	5.22612591E+06	3.56548458E-01	-8.95762875E+00	2.73373202E+01
97	8.70963590E+05	5.47242563E+06	3.61450935E-01	-8.83901295E+00	2.71038195E+01
98	9.12010839E+05	5.73033311E+06	3.66434066E-01	-8.72008316E+00	2.68689753E+01
99	9.54992586E+05	6.00039538E+06	3.71489459E-01	-8.60107010E+00	2.66313430E+01
100	1.00000000E+06	6.28318531E+06	3.76607944E-01	-8.48221047E+00	2.63898784E+01

2. - Tabulated Output for Measurement Condition Simulated Case

DISTRIBUTED FILTER WITH PARASITICS AND VOLTMETER LOADING

5 NODES 2 DISTRIBUTED SUBNETWORKS

1 GAIN ELEMENTS OF VCVS TYPE
NO. 1, SOURCE AT NODES 2 - 0, CONTROL VOLTAGE AT NODES 3 - 0, SUPRESS NODE 3, GAIN= 1.000000E+00

LUMPED ELEMENTS

NODES		R(OHMS)	C(FARADS)
1	4	1.000E+07	-0.
3	0	1.000E+07	-0.
3	0	-0.	2.500E-11
3	0	-0.	8.520E-12
4	0	-0.	8.520E-12

DISTRIBUTED NETWORK 1 50 SECTIONS CONNECTED TO NODES 4 3 5

TOTAL RESISTANCE= 2.16300000E+06 TOTAL CAPACITANCE= 8.23200000E-12

RESISTANCE/SECT.= 4.32600000E+04 CAPACITANCE/SECT.= 1.64640000E-13

DISTRIBUTED NETWORK 2 50 SECTIONS CONNECTED TO NODES 5 6 6

TOTAL RESISTANCE= 1.21500000E+05 TOTAL CAPACITANCE= 1.61800000E-18

RESISTANCE/SECT.= 2.43000000E+03 CAPACITANCE/SECT.= 3.23600000E-20

IX	FREQ(HZ)	RAD	VXM	VXM(DB)	PHASE(DEG)
1	1.04712855E+04	6.57930272E+04	1.81538888E-02	-3.48206066E+01	-1.41068716E+02
2	1.09647820E+04	6.88927569E+04	1.68933920E-02	-3.54456628E+01	-1.42947917E+02
3	1.14815362E+04	7.21406196E+04	1.57006044E-02	-3.60816725E+01	-1.44834842E+02
4	1.20226443E+04	7.55405023E+04	1.45735209E-02	-3.67287102E+01	-1.46727828E+02
5	1.25892541E+04	7.91006165E+04	1.35100992E-02	-3.73668292E+01	-1.48625287E+02
6	1.31827674E+04	8.28285137E+04	1.25082548E-02	-3.80560656E+01	-1.50525741E+02
7	1.38038426E+04	8.67321013E+04	1.15658593E-02	-3.87364419E+01	-1.52427839E+02
8	1.44543977E+04	9.08196593E+04	1.06807421E-02	-3.94279715E+01	-1.54330381E+02
9	1.51356125E+04	9.50998580E+04	9.85069372E-03	-4.01306637E+01	-1.56232328E+02
10	1.58489319E+04	9.95817762E+04	9.07347247E-03	-4.08445295E+01	-1.58132825E+02
11	1.65958691E+04	1.04274921E+05	8.34681220E-03	-4.15695872E+01	-1.60031196E+02
12	1.73780083E+04	1.09185246E+05	7.66843200E-03	-4.23058686E+01	-1.61926960E+02
13	1.81970086E+04	1.14335177E+05	7.03604678E-03	-4.30534256E+01	-1.63819822E+02
14	1.90546072E+04	1.19723628E+05	6.44737840E-03	-4.38123368E+01	-1.65709677E+02
15	1.99526231E+04	1.25366029E+05	5.90016691E-03	-4.45827141E+01	-1.67596596E+02
16	2.08929613E+04	1.31274348E+05	5.39218164E-03	-4.53647097E+01	-1.69480819E+02
17	2.18776162E+04	1.37461117E+05	4.92123167E-03	-4.61585238E+01	-1.71362741E+02
18	2.29086765E+04	1.43939440E+05	4.48517553E-03	-4.69644111E+01	-1.73242895E+02
19	2.39883292E+04	1.50723118E+05	4.08192983E-03	-4.77826893E+01	-1.75121933E+02
20	2.51188643E+04	1.57826479E+05	3.70947684E-03	-4.86137467E+01	-1.77000610E+02
21	2.63026799E+04	1.65264612E+05	3.36587077E-03	-4.94580512E+01	-1.78879758E+02
22	2.75422870E+04	1.73052253E+05	3.04924287E-03	-5.03161597E+01	1.79239736E+02
23	2.88403150E+04	1.81209044E+05	2.75780524E-03	-5.11887281E+01	1.77356950E+02
24	3.01995172E+04	1.89749163E+05	2.48985349E-03	-5.20765241E+01	1.75470957E+02
25	3.16227766E+04	1.98691765E+05	2.24376831E-03	-5.29804398E+01	1.73580843E+02
26	3.31131121E+04	2.08055820E+05	2.01801601E-03	-5.39015078E+01	1.71685732E+02
27	3.46736850E+04	2.17861188E+05	1.81114814E-03	-5.48409205E+01	1.69784814E+02
28	3.63078055E+04	2.28128670E+05	1.62180036E-03	-5.58000521E+01	1.67877362E+02
29	3.80189396E+04	2.38880043E+05	1.44869059E-03	-5.67804872E+01	1.65962758E+02
30	3.98107171E+04	2.50138112E+05	1.29061663E-03	-5.77840548E+01	1.64040509E+02
31	4.16869383E+04	2.61926759E+05	1.14645331E-03	-5.88128726E+01	1.62110269E+02
32	4.36515832E+04	2.74270986E+05	1.01514926E-03	-5.98694020E+01	1.60171855E+02
33	4.57088190E+04	2.87196980E+05	8.95723469E-04	-6.09565209E+01	1.58225260E+02
34	4.78630092E+04	3.00732156E+05	7.87261640E-04	-6.20776182E+01	1.56270666E+02
35	5.01187234E+04	3.14905226E+05	6.88912441E-04	-6.32367194E+01	1.54308452E+02
36	5.24807460E+04	3.29746252E+05	5.99883747E-04	-6.44386581E+01	1.52339201E+02
37	5.49540874E+04	3.45286714E+05	5.19438901E-04	-6.56893106E+01	1.50363708E+02
38	5.75439937E+04	3.61559576E+05	4.46893072E-04	-6.69959276E+01	1.48382977E+02
39	6.02559586E+04	3.78599354E+05	3.81609723E-04	-6.83676114E+01	1.46398231E+02
40	6.30957344E+04	3.96442192E+05	3.22997252E-04	-6.98160235E+01	1.44410915E+02
41	6.60693448E+04	4.15125936E+05	2.70505819E-04	-7.13566478E+01	1.42422714E+02
42	6.91830971E+04	4.34690219E+05	2.23624380E-04	-7.30096170E+01	1.40435589E+02
43	7.24435960E+04	4.55176539E+05	1.81877933E-04	-7.48043998E+01	1.38451857E+02

IX	FREQ(HZ)	RAD	VXM	VXM(DB)	PHASE(DEG)
44	7.58577575E+04	4.76628347E+05	1.44824999E-04	-7.67831293E+01	1.36474377E+02
45	7.94328235E+04	4.99091149E+05	1.12055311E-04	-7.90113511E+01	1.34506970E+02
46	8.31763771E+04	5.22612591E+05	8.31877175E-05	-8.15988158E+01	1.32555527E+02
47	8.70963590E+04	5.47242563E+05	5.78682942E-05	-8.47511864E+01	1.30631353E+02
48	9.12010839E+04	5.73033311E+05	3.57686384E-05	-8.89299518E+01	1.28764648E+02
49	9.54992586E+04	6.00039538E+05	1.65844392E-05	-9.56055842E+01	1.27098759E+02
50	1.00000000E+05	6.28318531E+05	1.55460346E-07	-1.36167607E+02	-1.57389654E+02
51	1.04712855E+05	6.57930271E+05	1.41472812E-05	-9.69865403E+01	-5.78943171E+01
52	1.09647820E+05	6.88937569E+05	2.61940233E-05	-9.16359558E+01	-5.95121334E+01
53	1.14815362E+05	7.21406196E+05	3.63311086E-05	-8.87944270E+01	-6.13016317E+01
54	1.20226443E+05	7.55405023E+05	4.47623518E-05	-8.69817421E+01	-6.31185756E+01
55	1.25892541E+05	7.91006165E+05	5.16749028E-05	-8.57344066E+01	-6.49330935E+01
56	1.31825674E+05	8.28285137E+05	5.72400990E-05	-8.48459925E+01	-6.67344109E+01
57	1.38038426E+05	8.67321013E+05	6.16143973E-05	-8.42063559E+01	-6.85172571E+01
58	1.44543977E+05	9.08196593E+05	6.49402962E-05	-8.37497147E+01	-7.02784597E+01
59	1.51356125E+05	9.50998580E+05	6.73472390E-05	-8.34336041E+01	-7.20158000E+01
60	1.58489319E+05	9.95817762E+05	6.89524969E-05	-8.32290000E+01	-7.37275447E+01
61	1.65958691E+05	1.04274921E+06	6.98620308E-05	-8.31151759E+01	-7.54122231E+01
62	1.73780083E+05	1.09189246E+06	7.01713275E-05	-8.30768061E+01	-7.70685059E+01
63	1.81970086E+05	1.14335177E+06	6.99662086E-05	-8.31022332E+01	-7.86951328E+01
64	1.90546072E+05	1.19723628E+06	6.93236083E-05	-8.31823768E+01	-8.02908639E+01
65	1.99526231E+05	1.25366029E+06	6.83123153E-05	-8.33100199E+01	-8.18544466E+01
66	2.08929613E+05	1.31274348E+06	6.69936775E-05	-8.34793236E+01	-8.33845924E+01
67	2.18776162E+05	1.37461117E+06	6.54222653E-05	-8.36654884E+01	-8.48799617E+01
68	2.29086765E+05	1.43939460E+06	6.36464916E-05	-8.39245106E+01	-8.63391562E+01
69	2.39883292E+05	1.50723118E+06	6.17091886E-05	-8.41930033E+01	-8.77607183E+01
70	2.51188643E+05	1.57826479E+06	5.96481382E-05	-8.44880621E+01	-8.91431379E+01
71	2.63026799E+05	1.65264612E+06	5.74965588E-05	-8.48071629E+01	-9.04848665E+01
72	2.75422870E+05	1.73053293E+06	5.52835477E-05	-8.51480819E+01	-9.17843392E+01
73	2.88403150E+05	1.81209044E+06	5.30344816E-05	-8.55088334E+01	-9.30400038E+01
74	3.01995172E+05	1.89749163E+06	5.07713775E-05	-8.58876211E+01	-9.42503571E+01
75	3.16227766E+05	1.98691765E+06	4.85132165E-05	-8.62827986E+01	-9.54139871E+01
76	3.31131121E+05	2.08055820E+06	4.62762337E-05	-8.66926399E+01	-9.65296213E+01
77	3.46736850E+05	2.17861188E+06	4.40741784E-05	-8.71163155E+01	-9.75961776E+01
78	3.63078055E+05	2.28128670E+06	4.19185482E-05	-8.75518753E+01	-9.86128173E+01
79	3.80189396E+05	2.38880043E+06	3.98188002E-05	-8.79982366E+01	-9.95789976E+01
80	3.98107171E+05	2.50138112E+06	3.77825437E-05	-8.84541761E+01	-1.00494520E+02
81	4.16869383E+05	2.61926759E+06	3.58157176E-05	-8.89185269E+01	-1.01359575E+02
82	4.36515832E+05	2.74270986E+06	3.39227561E-05	-8.93901774E+01	-1.02174772E+02
83	4.57088190E+05	2.87196980E+06	3.21067437E-05	-8.98680748E+01	-1.02941165E+02
84	4.78630092E+05	3.00732156E+06	3.03695641E-05	-9.03512288E+01	-1.03660258E+02
85	5.01187234E+05	3.14905226E+06	2.87120420E-05	-9.08387184E+01	-1.04333998E+02
86	5.24807460E+05	3.29746252E+06	2.71340800E-05	-9.13296980E+01	-1.04964752E+02
87	5.49540874E+05	3.45286714E+06	2.56347907E-05	-9.18234045E+01	-1.05555263E+02
88	5.75439937E+05	3.61559576E+06	2.42126232E-05	-9.23191631E+01	-1.06108598E+02
89	6.02559586E+05	3.78599354E+06	2.28654838E-05	-9.28163921E+01	-1.06628076E+02
90	6.30957344E+05	3.96442192E+06	2.15908500E-05	-9.33146052E+01	-1.07117190E+02
91	6.60693448E+05	4.15125936E+06	2.03858761E-05	-9.38134124E+01	-1.07579526E+02
92	6.91830971E+05	4.34690219E+06	1.92474900E-05	-9.43125179E+01	-1.08018672E+02
93	7.24435960E+05	4.55176538E+06	1.81724800E-05	-9.48117160E+01	-1.08438137E+02
94	7.58577575E+05	4.76628347E+06	1.71575703E-05	-9.53108842E+01	-1.08841273E+02
95	7.94328235E+05	4.99091149E+06	1.61994863E-05	-9.58099751E+01	-1.09231206E+02
96	8.31763771E+05	5.22612591E+06	1.52950074E-05	-9.63090062E+01	-1.09610783E+02
97	8.70963590E+05	5.47242563E+06	1.44410097E-05	-9.68080488E+01	-1.09982529E+02
98	9.12010839E+05	5.73033311E+06	1.36344981E-05	-9.73072169E+01	-1.10348622E+02
99	9.54992586E+05	6.00039538E+06	1.28726287E-05	-9.78066552E+01	-1.10710879E+02
100	1.00000000E+06	6.28318531E+06	1.21527224E-05	-9.83065284E+01	-1.11070760E+02

APPENDIX C

ELECTRONIC MATERIALS INC. BOULE EVALUATION

ELECTRONIC MATERIALS, INC.
P. O. Box 99
Sanatoga, Pennsylvania 19471
Telephone No. 215-326-7280

SILICON SLICE EVALUATION REPORT

Growth C 2

Crystal No. G 30-2

Type P

Customer Order No. 154206 67 Diameter: Minimum .949"

EMI Order No. _____ Maximum .952"

Number of pieces 336 Thickness: Minimum .008"

Resistivity .93 - 1.1 Maximum .0010"

Lifetime _____

Dopant Boron P

Orientation <111>

Finish Polished

EPD (5-point count system) < 2,000

Lineage NONE

Slippage NONE

REMARKS: Slices have been checked to an AQL of 4% on thickness parameter and defects.

Date: 8/8/68 Evaluation by: J W Vlahos

APPENDIX D

CLEANING

Cleaning of Silicon Prior to Oxidation[14]

1. Clean ultrasonically in trichlorethylene.
2. Rinse in acetone.
3. Copperplate in a solution of 200g $CASO_4$ and 10 ml. 48 per cent diluted to 1 liter with H_2O. This step omitted, instead the wafers were boiled in trichlorethylene for 30 minutes, then rinsed in methanol.
4. Rinse in deionized water.
5. Heat in nitric acid at 80° C for 20 minutes.
6. Flush in deionized water.
7. Boil in 30 per cent H_2O_2 for 10 minutes. This step omitted, instead the wafers were etched in 48 per cent HF until the acid no longer wets the silicon.
8. Flush in deionized water.

Cleaning of Tungsten Filament and Aluminum Prior to Evaporation[17]

1. Boil in trichlorethylene for 3 minutes.
2. Rinse in acetone.
3. Dry and load into vacuum.
4. Outgas filament by heating in vacuum to above evaporation temperature.
5. Boil aluminum charge in trichlorethylene, rinse in acetone, dry, and load into outgassed filament from 4.

APPENDIX E

PHOTO RESIST TECHNIQUE

Initial Condition of Substrate: Clean and Dry

1. Place substrate on photo-resist spinner.
2. Blow off any surface dust with research grade nitrogen.
3. Drop several drops of Shipley AZ1350 Photo Resist, which has been filtered through a Millipore type NR-WP-013-00 filter, onto the substrate.
4. Accelerate the wafer slowly (5 sec) to 2700 rpm.
5. Stop the rotation.
6. Reapply several more drops of filtered photo resist.
7. Accelerate the wafer rapidly to 2700 rpm and leave spinning for 30 seconds.
8. Stop the rotation and remove the wafer.
9. Dry the wafer for 5 minutes under a 250 watt infrared bulb at 12 inches above the substrate.
10. Expose resist through proper mask under a Sylvania "Sun Gun" type lamp of 625 watts at 12 inches for 15 seconds.
11. Develop the image in Shipley developer mixed according to label instructions for 5 seconds.
12. Stop the development quickly in water.
13. Dry the substrate by blowing it with research grade nitrogen.
14. Bake at 150° C in air if the etch is to be prolonged.

15. Etch as required.

16. Soak resist in remover which has been mixed according to label instructions until resist is removed, heating the remover as necessary.

APPENDIX F

ETCHES

Buffered Etch for SiO_2[16] (800Å/min)

40 gm NH_4F

60 ml H_2O

9 ml 48 per cent HF

Acidic Etch for Aluminum[18]

2 vol H_2O

1 vol HNO_3

1 vol Acetic Acid

16 vol Phosphoric Acid

APPENDIX G

EXPERIMENTAL DATA

Number	f_{null}, Khz	V_A, v	V_B, v	$\|G\|$, db	Q
1	130	9.230	16.930	-43	11.7
2	120	8.158	15.060	-43	13.0
3	119.5	7.513	13.962	-42	11.5
4	115	7.441	13.962	-40	10.0
5	100	5.548	10.436	-41	9.1
6	99	5.620	10.542	-41	10.0
7	99	5.548	10.436	-42	10.4
8	90	4.400	8.268	-41	9.5
9	89.1	4.039	6.981	-18	2
10	84.5	3.720	6.981	-40	9
11	80	3.152	5.828	-40	8.2
12	75	2.016	3.455	-39	8.5
13	71.5	2.000	2.760	-28	x
14	60	0.610	0.096	-38	6.1